# A Ku-Band Low-Phase-Noise Wide-Tuning-Range VCO in SiGe BiCMOS Technology

Xiangmin Li[1], Zhuang Kang[1], and Liang Jia[2]
[1] Yangtze University College of Arts and Sciences, Jingzhou 434020, China
[2] School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu 610054, China
Email: {limin_jinzhou, lxw_huang}@sina.com; fang_huangjiao6@163.com

***Abstract*** —In this paper, design and fabrication of a Ku-band voltage-controlled oscillator (VCO) using commercially available 0.18 μm SiGe BiCMOS technology is presented. To achieve the low phase noise, the VCO employs a $g_m$-boosted configuration which is a combination of cross coupled VCO and balanced Colpitts VCO, and the VCO simultaneously achieves wide tuning range. The tested results show that the VCO exhibits a phase noise of –116.2 dBc/Hz at a 1 MHz offset and presents a tuning range from 12.82 GHz to 14.28 GHz. The overall dc current consumption of the VCO is 2.1 mA with a supply voltage 1.8 V. The chip area of the VCO is 0.92×0.91 mm$^2$.

***Index Terms***—Voltage controlled oscillator, SiGe BiCMOS, Ku band, wide tuning range, low phase noise

## I. INTRODUCTION

Ku-band technology is increasingly finding roles in developing high resolution and compact radar systems. This is mainly because many aspects in a radar sensor, for instance, spatial resolution, antenna size, etc., are directly related to the wave-length of the adopted carrier signal. The resolution of a radar system can also be improved greatly by improving the tuning range (TR) and phase noise of the local oscillator used in the transceiver. Thus the necessity for a wide-tuning-range VCO with low phase noise is evident in the construction of high resolution radar sensor systems at Ku band.

The phase noise of a VCO near carrier frequency typically depends on the quality factor ($Q$) of the LC tank used in the oscillator and the noise of the active devices [1], [2]. The flicker noise (1/$f$) of the SiGe BiCMOS technology device is better than that of the CMOS or HEMT technology. Furthermore, SiGe BiCMOS is very attractive to be used for millimeter wave applications due to its reliable fabrication process and lower manufacturing cost [3], [4]. So, the SiGe BiCMOS technology is generally considered a good choice for low phase noise VCO design.

Manuscript received October 9, 2016; revised December 22, 2016.

This work was supported by by the National Basic Research Program of China (Grant No. 2012CBxx81xx), Advance Research project of China (Grant No. 58108xxxx01), and Advance Research Foundation of China (Grant No. 8340A09xxxx11DZ301).

Corresponding author email: limin_jinzhou@sina.com

doi:10.12720/jcm.11.12.1102-1105

The key factor associated with the phase noise for VCOs is the quality factor (Q) of its resonator, a two-time increase in Q will theoretically improve phase noise 6 dB. However, in integrated technology, there is limited room for Q improvement. When the Q-factor cannot be further improved, another key to phase noise reduction is the voltage swing and waveform shaping which are strongly related to the oscillator's circuit topologies. Several different topologies have been investigated. Two of the most common are cross coupled VCO [5], [7] and balanced Colpitts VCO [8], [9]. A combination of these two have also been proposed, the so-called $g_m$-boosted VCO [10]. The gm-boosted VCO has been demonstrated to have better phase noise attributed to substantial voltage swing and deep class-C operation with favorable impulse-sensitivity function. In this paper, a Ku-band low-phase-noise wide-TR $g_m$-boosted VCO is presented in 0.18 μm SiGe BiCMOS technology.

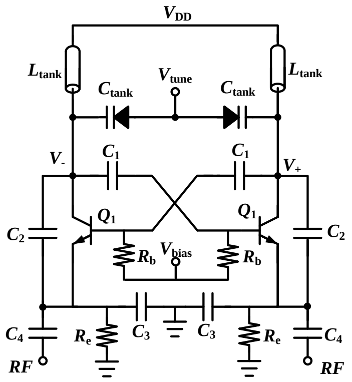


Fig. 1. Schematic of $g_m$-boosted VCO

## II. CIRCUIT DESIGN

The circuit schematic of $g_m$-boosted VCO is shown in Fig. 1, in which the inductors ($L_{tank}$) and the capacitors ($C_{tank}$) form the $LC$-resonating tank. A cross-coupled differential transistor pair ($Q_1$) with positive capacitive feedback ($C_1$) provide the necessary negative resistance to compensate the tank losses for sustaining oscillation. The capacitive voltage divider, composed of $C_1$ and $C_{BE}$ ($C_{BE}$ is the base-emitter junction capacitor of $Q_1$), is designed to approximately attain a loop gain of three in order to maximize the tank swing and simultaneously optimize the signal amplitudes at the base nodes to feed back from the collectors of $Q_1$. In order to further improve the phase noise of the VCO, a Colpitts configuration composed of $C_2$, $C_3$ and $C_4$ is inserted in the VCO. A simple resistor bias ($R_e$) provides a constant current for the VCO.

The frequency tuning range can be calculated by (1).

$$\Delta f = f_{\max} - f_{\min} = \frac{1}{2\pi\sqrt{LC_{\min}}} - \frac{1}{2\pi\sqrt{LC_{\max}}} \tag{1}$$

From Eq. (1), we can see that the bigger the ratio $C_{\max}/C_{\min}$ is, the wider the tuning range achieves. Considering this issue, a varactor array $C_{tank}$ consisting of seven BC diodes to have a large capacitance variation range is employed.

A collector-emitter feedback VCO, for instance, Colpitts or gm-boosted VCO, see Fig.1, requires a resistance $R_e$ at the emitter to provide a path for the dc bias current. This resistor should be large to avoid loading the tank severely and the relation is described as:

$$R_{tank} < R_e / n^2 \tag{2}$$

where $R_{tank}$ is the equivalent parallel resistance of the tank and $n$ is the capacitor ratio $n=C_2/(C_2+C_3)$. For instance, if the tank-impedance is $Z_C = \sqrt{L/C} = 10$ Ohm, the quality factor $Q$=20, and $R_{tank}$ is 200 Ohm. Then according to the transformation in (2), $R_e$ should be much larger than 50 Ohm to maintain the $Q$ factor. However, a current passing through the large resistance causes a voltage drop over $R_e$, therefore DC voltage at emitter is lifted which reduces the potential collector-emitter voltage swing at *RF* frequency ($V_{CE,RF}$). For the gm-boosted VCO in Fig. 1, the maximum *RF* voltage swing across collector-emitter can be expressed

$$V_{CE,RF,max} = V_{CC} - R_e I_{C0} - V_{knee} \tag{3}$$

where $V_{CC}$ is the collector bias voltage, $I_{C0}$ is the dc collector current and $V_{knee}$ is the knee voltage of the HBT. In order to reach the maximum *RF* swing, the transistor is usually biased with a high base voltage, which is around 3 times higher than the HBT turn-on voltage for a tank impedance $Z_c$=10 Ohm.

Although an oscillator is a strongly nonlinear circuit operated under large-signal conditions, an efficient method to quickly obtain the TR of the VCO is to start off with a small signal (*S*-parameter) analysis. Compared with transient or harmonic balance simulations, small-signal simulations are fast, do not suffer from nonconvergence problems, and do not require initial conditions. This is particularly important when simulating bipolar VCOs at millimeter-wave frequencies, and the transistor model must capture self-heating and avalanche multiplication, which are the positive feedback to cause significant nonconvergence problems at large voltage swings. During the transient simulations, the impedance of the *S*-parameter signal source is set to be a small value (i.e., 10 Ω-15 Ω), to clearly reflect the expected effective resistance of the tank inductance at the oscillation frequency, and thus to allow the onset of oscillations to occur.

As illustrated in Fig. 2, by plotting the real and imaginary parts of the impedance looking into the base of the HBT, $R_{in}$ and $X_{in}$, respectively, one can quickly assess if the circuit produces an adequate negative resistance at the desired oscillation frequency $f_{osc}$, (approximately the frequency at which $X_{in}$=0 and $R_{in}$<0 [1]), in turn to estimate the TR of the VCO. From Fig. 2, it can be concluded that $f_{osc}$ is about 13 GHz and 14.4 GHz when $V_{tune}$ is equal to 0 V and 1.8 V, respectively. Fig. 3 shows the simulated oscillation frequency of the VCO by the means of harmonic balance simulation, and it can be seen that the oscillation frequency range is from 13.2 GHz to 14.7 GHz, which is in accordance with that concluded with *S*-parameter analysis.

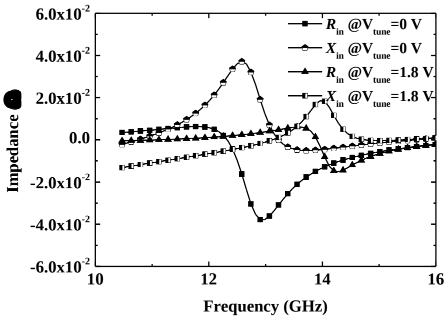


Fig. 2. Simulated input impedance as the tune voltage $V_{tune}$ is changed from 0 V to 1.8 V

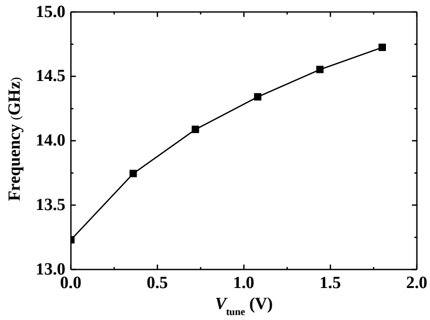


Fig. 3. Simulated oscillation frequencies of the VCO

## III. Measurement Results

The VCO was simulated using ADS2009U1 and fabricated in HHNEC 0.18 μm SiGe BiCMOS technology. The chip microphotograph of the VCO is illustrated in Fig. 4. The circuit occupies an area of 0.92×0.91 mm$^2$, including the bonding pads. The circuit was measured on wafer. The voltage and current source HP4142B was used to supply the dc voltages, meanwhile the output was connected through a Ground-Signal-Ground-Signal-Ground (GSGSG) probe to the spectrum analyzer Agilent N9030A and a 50 Ω load. The VCO was biased at $V_{DD}$=1.8 V ($I_{DD}$=2.1 mA ), consuming 3.78 mW of DC power.

TABLE I: COMPARISON OF HIGH-SPEED VCOS

| Ref. | $f_{osc}$ (GHz) | PN (dBc/Hz) | TR (%) | $P_{VCO}$ (mW) | Technology | $f_T/f_{max}$ (GHz) | FOM (dBc/Hz) |
|---|---|---|---|---|---|---|---|
| [11] | 23.1 | -94@1MHz | 5 | 2.5 | 0.18 μm SiGe BiCMOS | 120/135 | -177.3 |
| [12] | 20.89 | -97.2@1MHz | 10.5 | 40 | 0.13 μm SiGe BiCMOS | 100/130 | -167.6 |
| [13] | 24.27 | -100.3@1MHz | 2.2 | 7.8 | 0.18 μm CMOS | 90/- | -179.1 |
| [14] | 19 | -112@1MHz | 11 | 200 | 0.13 μm SiGe BiCMOS | 110/135 | -174.6 |
| This work | 13.6 | -116.2@1MHz | 10.7 | 3.78 | 0.18 μm SiGe BiCMOS | 120/135 | -193.1 |

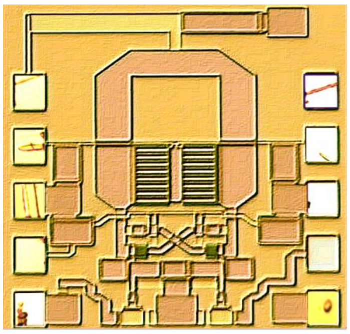

Fig. 4. Microphotograph of the VCO

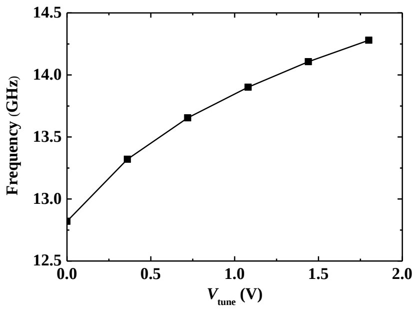


Fig. 5. Measured oscillation frequency of the VCO

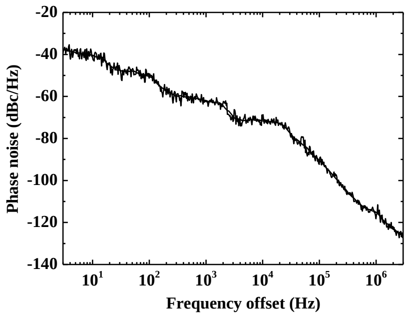


Fig. 6. Measured phase noise of the VCO

The oscillation frequency variation as a function of control voltage sweep is plotted in Fig. 5. The tuning frequency is varied from 12.82 GHz to 14.28 GHz with a control voltage from 0 to 0.18 V. It can be observed that the measured oscillation frequency (12.82 GHz-14.28 GHz) of the VCO is slightly shifted down as compared to the simulated oscillation frequency (13.2 GHz-14.7 GHz). The difference between the simulated and measured results can be attributed to the reason that all the passive elements and wirings of circuit were modeled by quasi 3-D electromagnetic simulations of momentum electromagnetic (EM) simulator in Agilent's Advanced Design System (ADS). It is difficult to set the substrate parameters to be as same as the fabricated due to the deviation of actual process from the list in the library.

The phase noise of the VCO is difficult to measure, due to the spectrum jittering caused by the noise from the supply and tuning voltages. In this work, the phase noise is roughly measured using the Phase Noise Utility of the spectrum analyzer (Agilent N9030A). Fig. 6 shows the measurement results, in which the phase noise of the VCO is -116.2 dBc/Hz at 1 MHz offset from the carrier frequency 13.6 GHz, which is lower than that in other wide-TR VCOs.

Table I shows the comparison of the performance of the designed VCO in this paper with the previously reported high-speed VCOs [11]-[14]. The commonly used figure of merit (FOM) parameter, which accounts for phase noise (PN), oscillation frequency ($f_{osc}$), frequency offset ($\Delta f$) from $f_{osc}$, and power dissipation ($P_{VCO}$) as depicted in (4), is used for the comparison. As can be seen from Table I, The VCO reported in this work has an excellent FOM comparing with the other oscillators processed in SiGe BiCMOS, or CMOS technology.

$$\mathrm{FOM} = \mathrm{PN} - 20\log\left(\frac{f_{osc}}{\Delta f}\right) + 10\log\left(\frac{P_{VCO}}{1\mathrm{mW}}\right) \quad (4)$$

## IV. CONCLUSIONS

In this paper, a Ku-band VCO in 0.18 μm SiGe BiCMOS technology has been presented. To achieve wide TR and low phase noise, the VCO was implemented using the structure of $g_m$-boosted VCO. By introducing a small signal (*S*-parameter) analysis method the design process of the VCO is accelerated. Measured results show that the VCO has achieved an oscillation frequency range from 12.82 GHz to 14.28 GHz (10.7%). The phase noise is -116.2 dBc/Hz at 1-MHz offset from the center oscillation frequency 13.6 GHz. The FOM achieves -193.1 dBc/Hz.


## ACKNOWLEDGMENT

This work was supported by the National Basic Research Program of China (Grant No. 2012CBxx81xx), Advance Research project of China (Grant No. 58108xxxx01), and Advance Research Foundation of China (Grant No. 8340A09xxxx11DZ301).

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**Xiang-min Li** was born in Hubei Province, China, in 1981. He received the B.S. degree from the College of Electronic Information Engineering, Yangtze University, in 2005. His research interests include circuit design and array signal processing.

**Zhuang Kang** was born in Hubei Province in 1987 and graduated from Hubei Automotive Industry Institute in 2010. His major research interests include communication and information system, signal and information processing, integrated circuit engineering

**Liang Jia** was born in Sichuan Province, China, in 1990. He received the B.S. degree from University of Electronic Science and Technology of China, Chengdu, in 2015. His research interests include RF circuit design and radar signal processing.