An Efficient Digital Code Shifted Reference (CSR) Based UWB Transceiver on FPGA Platform

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Abstract—The Ultra-wideband (UWB) system is a wireless technology that offers flexible data rate with better energy efficiency and is used for short-range communications. The Code-shifted-reference (CSR) UWB radio uses the Walsh codes technique to distinguish between the data pulse and reference pulse sequences. The Code-shifted-reference (CSR) UWB transceiver is designed at different code lengths in this manuscript. The CSR-UWB Transmitter is designed using shifting and reference codes, data frame, and pulse generation units. The CSR-UWB receiver is designed using an autocorrelator, data detection, and decoder unit. The data detection unit performs detection and synchronization mechanisms to improve the chip area. The CSR-UWB transceiver is designed and implemented on Artix-7 FPGA on Xilinx environment using Verilog HDL. The CSR-UWB transceiver utilizes the < 1% chip area (Slices) and operates at 267.236 MHz by consuming the total power of 103 mW on Artix-7 FPGA. The CSR-UWB transceiver achieves a throughput of 27.4 Mbps, 356.98 Mbps, and 713.95 Mbps at code lengths 2, 4, and 8, respectively. The hardware efficiency of 0.61 Mbps/Slice, 6.99 Mbps/Slice and 12.1 Mbps/Slice is obtained at code lengths 2, 4, and 8, respectively using proposed Transceiver. The performance metrics like chip area, frequency, power, and throughput of the proposed CSR-UWB transceiver are improved compared to those of existing CSR-UWB transceivers and other PHY transceiver designs.

Keywords—code-shift-reference, ultra-WideBand, FPGA, transceiver, pulse generation

I. Introduction

Short-distance communication is one significant domain in advanced wireless technology due to higher demand in the Internet of Things (IoT) field and mobile communications. The Narrowband (NB) and Ultra-wide-band (UWB) are two Radio frequency (RF) based wireless standards. The current narrowband wireless standards like Zigbee, Bluetooth, and Wi-Fi devices are failed to meet the demands of the next-generation communication system. The devices like Zigbee and Bluetooth offers low data rate within 2 Mbps and drastically degrades the system performance by utilizing more power. In contrast, the Wi-Fi system offers a better data rate of up to Gigabits per second (Gbps). It has a complex architecture, which increases the power consumption and latency of the system. The UWB wireless technology offers better data rates, high range accuracy, and good energy efficiency than NB standards [1]. The signal bandwidth of the UWB is greater than 500 MHz. The power spectral density (PSD) of the UWB system is 41.3 dBm/ MHz for inherent noise. The UWB acts as an interface mechanism for high-data rate transmission in wireless applications under IEEE 802.15.4a standards. The impulse Radio-UWB (IR-UWB) and frequency modulation (FM-UWB) is two UWB data transmission approaches [2].

The IR-UWB architecture is simple and offers low power with better system performance due to high channel capacity. The UWB can avoid the multipath effects and spatial diversity to improve the system's accuracy. The UWB is used in most wireless applications as a communication interface, including Wireless Body area networks (WBANs) and Wireless Personal Area Networks (WPANs). The UWB technology is used in medical sensing and transmission system, including capsule endoscopy and medical radar [3]. The IR-UWB receivers are classified into two types based on channel capacity: one is coherent, and the other is non-coherent type. The non-coherent IR-UWB receivers are divided into traditional autocorrelation, modified autocorrelation, special non-coherent type, and energy detector receivers [4, 5]. The Transmitter-reference (TR) based UWB receiver provides low-complexity features and the ability to detect the data symbols at a lower data rate without using channel estimation coefficients. The TR-UWB receiver uses the synchronization algorithm to improve the Bit error rate (BER) at different channel conditions [6].

The Code-shifted-reference (CSR) UWB radio separates the data pulse and reference pulse sequences with coding mechanisms like Walsh codes. The shifting and detection coding mechanism is introduced to remove the UWB delay element and group of analog carriers in TR-based UWB and frequency-shifted reference (FSR)

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based UWB systems, respectively. The CSR-UWB transceiver offers a low-complexity design with better BER performance than TR and FSR-UWB-based transceiver architectures [9]. The differential CSR (DCSR)-UWB transceiver is introduced to reduce the transmitted power of the reference pulse sequences. The CSR and DCSR offer good performance with lesser system complexity [10, 11]. Internally coded time hopping approach is introduced in the CSR-UWB system to realize the performance metrics with BER improvement than uncoded CSR-UWB system [12]. The UWB Technology is used for low-data rate applications like WBANS, WPANs, and medical sensing-transmission systems. UWB Technology supports home network applications like digital video, audio, and internet with suitable data rates.

The efficient CSR-UWB Transceiver architecture is designed in this manuscript. The contribution of the work is as follows: The proposed CSR-UWB transceiver offers low-latency and high-throughput architecture and is used in most UWB applications. The transceiver is designed at different code lengths and offers better hardware efficiency. The proposed design provides better performance metrics than the other CSR-UWB TR and existing PHY TRs. Most of the existing UWB systems use a barker identifier as a decoding mechanism with a synchronizer to decode the final output, which affects the chip area and efficiency of the UWB system. The proposed CSR-UWB system uses a simple decoding mechanism, which identifies and compares the auto-correctors output with data detection codes to improve the performance metrics.

The manuscript's organization is as follows: Section II discusses the existing works of the UWB transceiver architectures and their performance metrics. The proposed CSR-UWB transceiver architecture is explained in Section III. The results and discussion of the proposed work with performance comparison are analyzed in Section IV. The overall work is concluded in Section V with the futuristic suggestion.

II. Literature Review

Strackx et al. [13] presented the electromagnetic (EM) subtraction-based flexible UWB pulse transmitter on a Field Programmable Gate array (FPGA) platform. The EM subtraction approach provides highly flexible doublets, monocycles, and gaussian based pulses in a single chip of FPGA. The work analyses the pulses concerning the time, voltage, and frequency. The EM-based approach is a better alternative to the digital clock manager (DCM) on the FPGA platform, with easy implementation and flexibility features. Olonbayar et al. [14] describe the impulse Radio (IR)-UWB baseband Transceiver implementation on both Application-specific Integrated Circuit (ASIC) and FPGA platforms for IEEE 802.15.4a applications. The synchronization-mechanism performs better even in large distortion conditions in the architecture. The packet reception performance is analyzed under uncoded and coded conditions. The baseband architecture supports up to 27.24 Mbps by consuming 74 mW power on the ASIC platform. Shimizu et al. [15] explained the IR-UWB receiver architecture to realize the performance-of-body-Out-of-body communication. The receiver architecture contains memory, synchronization, and detection units. The IR-UWB transceiver is connected to the Liquid Photom to realize the performance metrics with real-time setup. The work offers a data rate of 2 Mbps with a BER of 10-3 and covers a distance of up to 70 mm.

Jin et al. [16] presented the Transmitted reference (TR) based UWB Transceiver with non-ideal delay lines (DL). The group delay-ripple (GDR) of DL produces the distortions. This work improves the distortions using a non-ideal DL-based approach in the receiver unit. The work evaluates the BER under different signal-to-noise ratio (SNR) and GNR ratio conditions and compares it with the conventional approach. Sheth et al. [17] explained the IR UWB receiver and its performance comparison. The different IR-UWB receivers like CSR, Multi-differential Frequency shift reference (MF-DSR), and Transmitted reference (TR) were considered pulse-transmitting approaches in the UWB communication system. The work analyses the Bit error rate (BER) against signal-to-noise ratio (SNR) by concerning the number of frames (Nf) and several shift codes (M) for all three-IR-UWB receivers. The CSR-based approach provides better BER than the other two approaches, TR and MF-DSR approaches. Shanthi et al. [18] described the Frequency synthesizer module for multiband-Orthogonal frequency division multiplexing (MB-OFDM) based UWB transceivers. The delay-locked loop (DLL) based frequency synthesizer reduces the design complexity rather than the phase-locked loop (PLL) based approach. The work analyses the energy, delay, data rate, and static power at different traffic levels. Jayaprakash et al. [19] presented the differential-CSR (DCSR) encoder and decoder mechanism for UWB transceivers. The DCSR method utilizes less power than CSR and transmits the reference codes free differential encoded data to the receiver unit. This work analyses CSR and DCSR-based approaches on FPGA and realizes the chip area and throughput at different data widths. Qiu et al. [20] explained the adaptive beam approach for UWB impulse transceivers. The transceiver includes a driver amplifier, pulse generator, PLL, DLL voltage-controlled oscillator, switch, charge pump, and buffer units. The work analyses the transmitted, detected, recovered, and PLL tuned pulses. The TX and RX consume total power of 67 mW and 151 mW, respectively, using 180 nm CMOS technology. Schmidt et al. [21] described the wireless connectivity issues and enabling the UWB in the aerospace industry. There are many challenges like network performance targets, security, ambiance energy operation, and coexistence with other systems. The latency and throughput trade-off, the impact of deployment position, and lifetime and sustainability features are improved by enabling the UWB technology.

Jaglan et al. [22] presented the Circular monopole UWB antenna design with triple band notches using the Electromagnetic band gaps (EBG) framework. The work discusses the Voltage standing wave ratio (VSWR) against frequency and its effects using different EBG frameworks.

With the continuation, the Dual band EBG framework based UWB multi-input-Multi-Output (MIMO) antenna is designed with wide band electromagnetic coupling effects reduction [23]. The UWB MIMO antenna with triple band notches is realized to enhance the wideband isolation using Uniplanar and mushroom EBG framework [24]. Dharmarajan et al. [25] discussed the Human face-shaped (HFS) based dual-polarized MIMO UWB antenna with high resolution and gain features. The MIMO antenna bandwidth (2.8–16.1 GHz) covers the UWB system by removing the Wireless Local area network (WLAN) signals ranging from 5 to 6.4 GHz.

Hennessy et al. [26] presented the digital CSR UWB transmitter (TX) and receiver (RX) architecture with security features on both FPGA and ASIC platforms. The security key is added with reference codes in the transmitter unit for key rotation. The receiver architecture introduces the autocorrelator, detector, synchronizer, and decoder units. The work considers floating-point and fixed-point representations to implement the TX and RX on FPGA. The design module operates at 82 MHz, consuming a total power of 0.63 mW on-32 nm CMOS Technology.

III. Digital CSR Based UWB Transceiver

The orthogonal shifting codes are used to separate the data signals from the reference signal on both transmitter (TX) and receiver (RX) sides during communication. The TX and RX modules mutually agreed to use shifting and reference codes during communication establishment. It will be easy to detect and decode the original input data signal. These shifting and reference codes have constructed a series of either positive or negative ones. The Code-shifted-reference (CSR) approach has used these codes to shift data orthogonally to detect the original input data by satisfying the below three Eq. (1–3) as follows[7]:

$$\sum_{i=0}^{N_f-1} c_{ip} = 0, \quad \forall p \in \{0,1,2,\dots,M\} \tag{1}$$

$$\sum_{i=0}^{N_f-1} r_{i0}\, c_{ip}\, s_{il} \begin{cases} 0, & if\ (p \neq l), \\ N_f, & if\ (p = l), \end{cases} \quad \forall p,l \in \{0,1,2,,M\} \tag{2}$$

$$\sum_{i=0}^{N_f-1} s_{il}\, c_{ip}\, s_{in} = 0, \quad \forall p,l,n \in \{0,1,2,\dots,M\} \tag{3}$$

where c_{ip} is the detection code, r_{i0} is the reference code, and s_{il} and s_{in} are possible shifting codes. N_f denotes the number of frames, and the number of bits grouped with reference codes is denoted by M. The idea of multiple detection codes produces better outcomes by continuously changing reference and shifting codes using the above equations. Shifting the data bits from the reference codes in the CSR approach is compulsory to detect the original data using detection codes. The reference codes are multiplied with waveform samples to generate the reference sample and are orthogonal. The data and reference signals are added in the time domain and are separated in the CSR coding approach. The shifting and reference codes use a set of orthogonal codes called Walsh codes. The selection of shifting and detection codes under different code lengths in the CSR approach is tabulated in Table I. The code length varies from 2 to 8 based on the selection of shifting and reference codes in CSR-UWB TX and RX. The detection codes are used in RX to recover the original input data. The reference code at code length eight for CSR-UWB Transceiver is represented in Eq. (4) as follows [9]:

$$\begin{bmatrix} r_0 \\ r_1 \\ r_2 \\ r_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ -1 & -1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \end{bmatrix} \tag{4}$$

The CSR-based UWB transceiver (TR) architecture is illustrated in Fig. 1. The CSR-UWB TX has shifting codes, reference codes, a data framing unit (DFU), a pulse generator, adders, and multipliers. The CSR-UWB RX has detection codes, a data detection unit (DDU), an autocorrelator unit, a decoder unit, and a data register. In this work, three different CSR-UWB TX and RX modules are designed based on code lengths (N_f) like 2, 4, and 8. The CSR-UWB TX and RX modules use the corresponding shifting, reference, and detection codes based on code lengths. The CSR-UWB TR module is designed for different data widths like 1, 2, and 4 using code lengths 2, 4, and 8, respectively.

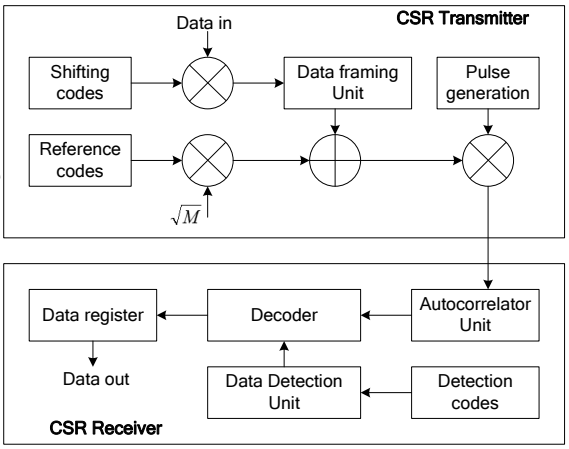

Figure 1. The architecture of the CSR-based UWB transceiver

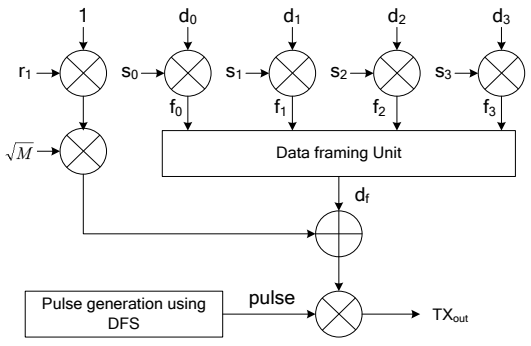

Figure 2. Hardware architecture of the CSR based UWB transmitter

The hardware architecture of the CSR-based UWB transmitter at code length eight is illustrated in Fig. 2. The transmitter receives four-bit input data values, and are

multiplied individually with shifting codes (s_0, s_1, s_2, and s_3). These 1-bit input data values are either positive or negative ones. The multiplied results are stored individually in the data framing unit (DFU).

The reference code (r_1) is selected from Eq. (4) of the 2nd row and is multiplied with the initial value one. The results are again multiplied with the initial value. The corresponding code lengths 2, 4, and 8 in the CSR-based UWB transceiver. The DFU receives all the multiplied values individually and processes the data framing according to the input values. The DFU process in the CSR-UWB transmitter is tabulated in Table II. The f_0, f_1, f_2, and f_3 are the shifted data outputs generated using data inputs and shifting codes. The DFU selects the corresponding framed output (d_f) based on the input data values. The framed output is added with reference output to generate the single frame output. The digital frequency synthesizer (DFS) generates the pulses at a 10 MHz frequency. The frame output is multiplied with pulses to generate the CSR-UWB transmitter output (TX_{out}) in a sequence. The CSR-UWB Transmitter is constructed using Eq. (5) as follows [9]:

$$TX_{out} = \left(\left(r_1 . \sqrt{M} \right) + d_f \right) . pulses \quad (5)$$

TABLE I. SELECTION OF SHIFTING AND DETECTION CODES UNDER DIFFERENT CODE LENGTHS

Code Length (N)	Shifting Codes	Detection Codes
2	$s_0 = [\ 1\ \ -1\ ]$	$c_0 = [\ 1\ \ -1\ ]$
4	$s_0 = [1\ \ -1\ \ -1\ \ 1\ ]$ $s_1 = [1\ \ -1\ \ 1\ \ -1\ ]$	$c_0 = [1\ \ -1\ \ 1\ \ -1\ ]$ $c_1 = [1\ \ -1\ \ -1\ \ 1\ ]$
8	$s_0 = [1\ \ -1\ \ -1\ \ 1\ \ 1\ \ -1\ \ -1\ \ 1\ ]$ $s_1 = [1\ \ -1\ \ 1\ \ -1\ \ 1\ \ -1\ \ 1\ \ -1\ ]$ $s_2 = [1\ \ -1\ \ -1\ \ 1\ \ -1\ \ 1\ \ 1\ \ -1\ ]$ $s_3 = [1\ \ -1\ \ 1\ \ -1\ \ -1\ \ 1\ \ -1\ \ 1\ ]$	$c_0 = [1\ \ -1\ \ 1\ \ -1\ \ -1\ \ 1\ \ -1\ \ 1\ ]$ $c_1 = [1\ \ -1\ \ -1\ \ 1\ \ -1\ \ 1\ \ 1\ \ -1\ ]$ $c_2 = [1\ \ -1\ \ 1\ \ -1\ \ 1\ \ -1\ \ 1\ \ -1\ ]$ $c_3 = [1\ \ -1\ \ -1\ \ 1\ \ 1\ \ -1\ \ -1\ \ 1\ ]$

TABLE II. DFU PROCESS IN CSR-UWB TRANSMITTER

Data inputs [d_3, d_2, d_1, d_0]	Framed outputs (d_f)	Data inputs [d_3, d_2, d_1, d_0]	Framed outputs (d_f)
[-1 -1 -1 -1]	$f_3 + f_2 + f_1 + f_0$	[1 -1 -1 -1]	$f_2 + f_1 + f_0$
[-1 -1 -1 1]	$f_3 + f_2 + f_1$	[1 -1 -1 1]	$f_2 + f_1$
[-1 -1 1 -1]	$f_3 + f_2 + f_0$	[1 -1 1 -1]	$f_2 + f_0$
[-1 -1 1 1]	$f_3 + f_2$	[1 -1 1 1]	f_2
[-1 1 -1 -1]	$f_3 + f_1 + f_0$	[1 1 -1 -1]	$f_1 + f_0$
[-1 1 -1 1]	$f_3 + f_1$	[1 1 -1 1]	f_1
[-1 1 1 -1]	$f_3 + f_0$	[1 1 1 -1]	f_0
[-1 1 1 1]	f_3	[1 1 1 1]	-1

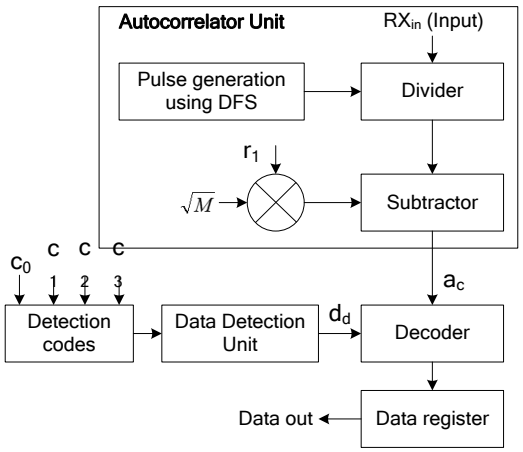

Figure 3. Hardware architecture of the CSR based UWB receiver

The hardware architecture of the CSR based UWB Receiver is illustrated in Fig. 3. The CSR-UWB receiver has mainly three units: autocorrelator, data detection, and decoder units. The autocorrelator receives the transmitted output (TXout) and divides with pulses. The reference output is subtracted from the divider output to generate the autocorrelator output (a_c). The autocorrelator output (a_c) generates the outcome simultaneously due to the received transmitted output being obtained based on shifting and reference codes. The detection codes (c_0, c_1, c_2, and c_3) detect the original input data. The data detection unit (DDU) receives the detection codes in a framed format, as mentioned in Table III generates the 16 possible framed outcomes (d_d).

TABLE III. DATA DETECTION UNIT (DDU) PROCESS FOR DECODER

Detection code	DDU Output (d_d)	Detection code	DDU Output (d_d)
-1	dd_0	c_3	dd_8
c_0	dd_1	$c_3 + c_0$	dd_9
c_1	dd_2	$c_3 + c_1$	dd_{10}
$c_3 + c_2$	dd_3	$c_3 + c_1 + c_0$	dd_{11}
c_2	dd_3	$c_3 + c_2$	dd_{12}
$c_2 + c_0$	dd_5	$c_3 + c_2 + c_0$	dd_{13}
$c_2 + c_1$	dd_6	$c_3 + c_2 + c_1$	dd_{14}
$c_2 + c_1 + c_0$	dd_7	$c_3 + c_2 + c_1 + c_0$	dd_{15}

The DDU integrates the detection codes to find the frame boundaries. The decoder receives autocorrelator output (a_c) and DDU outcomes (d_d) for the decoding mechanism. The decoder identifies the correct outcomes by comparing the autocorrelator output (a_c) and DDU outcomes (d_d). If the autocorrelator output (a_c) is equal to the first possible outcome (d_d) of the DDU, then the decoder identifies the original output as -1 [1 1 1].

Similarly, If the autocorrelator output (ac) is equal to eight possible outcomes (000 to 111) of the DDU, then the decoder identifies the original output as [1 1 1 1]. The decoder identifies the corresponding outcomes until the user stops sending the input data. Lastly, the data register stores the decoder output and is considered as CSR-UWB RX output. The RX output values must match with TX original input data values to verify the complete CSR-UWB TR is working correctly.

IV. Results and Discussion

The digital CSR-UWB transceiver module results are discussed in this section. The CSR-UWB transceiver and sub-modules are synthesized and implemented on Artix-7 (XC7A100-T CSG324) FPGA. The CSR-UWB transceiver module is designed using Verilog HDL on the Xilinx environment. The performance results of CSR-UWB Transmitter, Receiver, and Transceiver modules at different code lengths are analyzed. The chip area (Slices, Lookup Tables (LUTs), LUT-Flip-flops (FFs)), maximum operating frequency, total power, latency, throughput, and hardware efficiency are considered for performance realization. Lastly, the proposed designs are compared with existing approaches with better improvements in performance metrics.

The resource utilization of Digital CSR-UWB Transceiver (TR) at different code lengths (Nf) on Artix-7 FPGA is tabulated in Table IV. The CSR-UWB TR utilizes slices of 45 and LUTs of 530 and operates at a frequency of 41. 085 MHz at code length two. Similarly, the CSR-UWB TR utilizes the slices of 51, LUTs of 588, and operates at a frequency of 267.73 MHz at code length four. The CSR-UWB TR utilizes the slices of 59, LUTs of 929, and operates at a frequency of 267.73 MHz at code length eight. The combinational logic is used in most parts for designing the internal architecture of the CSR-UWB-RX with code length two than the sequential circuits, which lowers the frequency and consumes more power. So, the Overall CSR-UWB TR using code length two works at a lower frequency than the other two designs.

The CSR-UWB TR consumes the total power of 98 mW, 99 mW, and 103 mW at code lengths of two, four, and eight, respectively. The CSR-UWB TR uses only 1.5 clock cycles as latency to execute the design at code lengths. The throughput of the design is calculated using data input width, latency, and operating frequency parameters. The CSR-UWB TR obtains the throughput of 27.4 Mbps, 356.98 Mbps, and 713.95 Mbps at code lengths of two, four, and eight, respectively. The hardware efficiency is determined based on throughput per slice; its unit is Mbps/slice. The 12.1 Mbps/slice efficiency is obtained for CSR-UWB TR at code length eight on Artix-7 FPGA.

The resource utilization of the digital CSR-UWB transmitter (TX) and receiver (RX) modules on Artix-7 FPGA is tabulated in Table V. The CSR-UWB TX module utilizes < 1 % chip area (Slices and LUTs) and operates at 267.236 MHz at different code lengths. The CSR-UWB TX module utilizes < 1 % slices and 1 % LUTs at different code lengths on Artix-7 FPGA. The graphical representation of resource utilization for Digital CSR-UWB TR and its sub-modules are illustrated in Fig. 5. The power consumption of all the design modules is realized using the Xilinx Xpower analyzer at a

TABLE IV. Resource Utilization of Digital CSR-UWB Transceiver at Different Code Lengths on Artix-7 FPGA

Resources	N_f = 2	N_f = 4	N_f = 8
Chip area and Frequency			
Slices	45	51	59
LUTs	530	588	929
LUT-FFs	44	49	58
Max. frequency (MHz)	41.085	267.73	267.73
Power			
Dynamic power (mW)	16	17	21
Total power (mW)	98	99	103
Performance			
Latency (CC)	1.5	1.5	1.5
Throughput (Mbps)	27.4	356.98	713.95
Efficiency (Mbps/Slices)	0.61	6.99	12.1

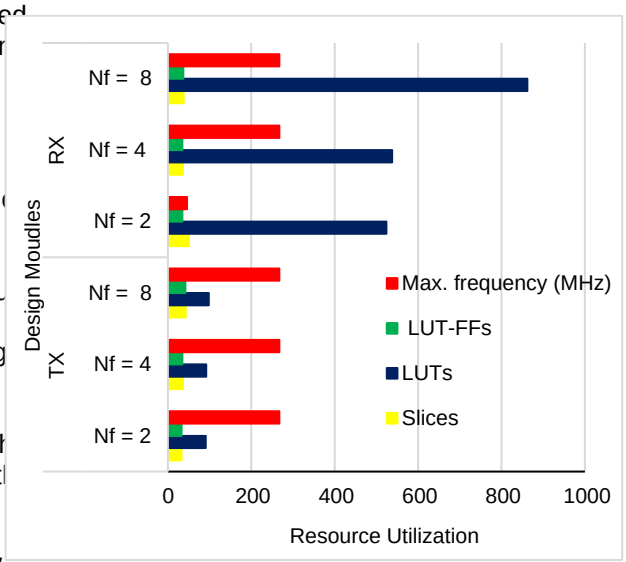

Figure 4. Graphical representation of resource utilization for Digital CSR-UWB TR

TABLE V. Digital CSR-UWB Transmitter and Receiver Utilization on Artix-7 FPGA

Code Lengths	Slices	LUTs	LUT-FFs	Frequency (MHz)
TX				
N_f = 2	33	91	33	267.236
N_f = 4	36	92	35	267.236
N_f = 8	43	98	42	267.236
RX				
N_f = 2	50	524	35	45.837
N_f = 4	36	538	35	267.236
N_f = 8	38	862	37	267.236

The total power consumption representation of the

clock frequency of 100 MHz. The CSR-UWB TX consumes the total power from 87 to 89 mW at different code lengths. Similarly, the CSR-UWB RX consumes the total power from 93 to 99 mW at different code lengths on Artix-7 FPGA. The CSR-UWB TR consumes the total power from 98 to 103 mW at different code lengths on Artix-7 FPGA.

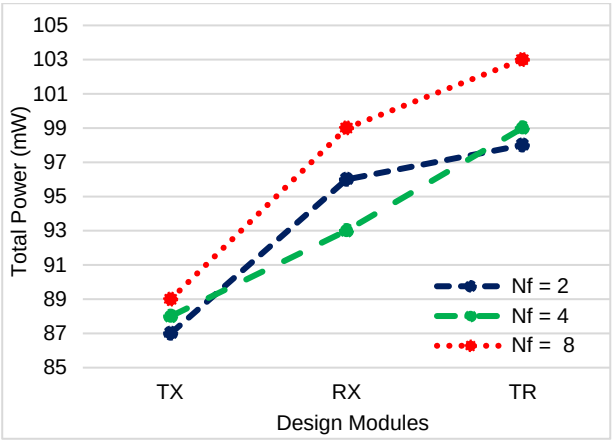

Figure 5. Total power consumption representation of the digital CSR-UWB TR and its modules

The performance comparison of the proposed Digital CSR-UWB TX and RX with the existing approach [26] is tabulated in Table VI. The existing CSR-UWB TX and RX modules are designed with fixed-point representation and implemented on Spartan-6 FPGA. The CSR-UWB RX module is constructed with an auto-correlator, synchronizer, detector, and decoder units. The proposed CSR-UWB TX provides less resource utilization overhead by concerning 75.84 % of slices, 75.12 % of LUTs, operating at a high frequency of 36.41 %, and high throughput of 36.19 % than the existing CSR-UWB TX module [26]. Similarly, the proposed CSR-UWB RX provides less area overhead concerning 92.85 % of slices and 17.48 % of LUTs, operating at a high frequency of 55.43 % and high throughput of 55.21 % than the existing CSR-UWB RX module [22]. Overall, the proposed CSR-UWB TX and RX modules provide better performance metrics than the existing CSR-UWB TX and RX modules [26].

The performance comparison of the proposed work with existing different physical layer (PHY) TR implementations [27 32] is tabulated in Table VII. The type of FPGA, design approach, type of physical layer used, chip area, frequency, and power parameters are considered for performance comparison. The Narrowband (NB) PHY-baseband TR is designed using BCH codes for IEEE 802.15.6 Wireless Body area network (WBAN) applications on Virtex-6 FPGA. The proposed CSR-UWB TR offers less area overhead in terms of 28.15 % LUTs, operating at a high frequency of 77.52 %, and consumes less power of 36.41 % than the existing NB-PHY TR module [27]. The Impulse radio (IR) based UWB TR is designed using Discrete Wavelet Packet Transform (DWPT) approach for bio-sensor applications on Virtex-7 FPGA. The proposed CSR-UWB TR offers less area overhead in LUTs of 72.65 %, operating at a high frequency of 62.92 %, and consumes less power of 9.65 % than the existing IR-UWB TR module [28].

The digital capsule endoscope-based Human body communication (HBC) TR is designed using the Frequency selective digital transmission (FSDT) method as per IEEE 802.15.6 standards for Health monitoring applications on Artix-7 FPGA. The proposed CSR-UWB TR offers less area overhead in LUTs of 82.24 %, operating at a high frequency of 88 %, and consumes less power of 9.65 % than the existing HBC-PHY TR module [29]. The IEEE 802.15.4-based PHY TR is designed using offset-Quadrature phase shift keying (O-QPSK) modulation approach for wireless personal area network (WPAN) applications on Artix-7 FPGA. The proposed CSR-UWB TR offers less area overhead in LUTs of 34.94 % and consumes less power, 39.76 %, than the existing PHY-TR module [30].

The PHY-based digital TR (DTR) is designed using IEEE 802.3 standard for body coupled communication (BCC) applications on Artix-7 FPGA. The proposed CSR-UWB TR offers less area overhead in LUTs of 63.09 %, operates at a high frequency of 13.1 %, and consumes less power of 8.84 % than the existing PHY-DTR module [31]. The HBC-PHY TR is designed using the FSDT approach as per IEEE 802.15.6 standards for WBAN applications on Artix -7 FPGA. The proposed CSR-UWB TR offers less area overhead in slices of 69.89 % and LUTs of 8.11 %, operating at a high frequency of 4.11 % than the existing HBC-PHY TR module [32].

The CSR-UWB Transceiver offers low-latency and high throughput features, which are flexible to incorporate any standard wireless applications, especially WPANs. The architecture of the CSR-UWB TR with code length two has to improve concerning the frequency and efficiency parameters.

TABLE VI. PERFORMANCE COMPARISON OF PROPOSED DIGITAL CSR-UWB TX AND RX WITH EXISTING APPROACH [26]

Resources	CSR-UWB TX [26]	Proposed TX	CSR-UWB RX [26]	Proposed RX
FPGA	Spartan-6	Spartan-6	Spartan-6	Spartan-6
Slices	207	50	728	52
LUTs	394	98	875	722
DSPs	1	1	10	0
Frequency (MHz)	117	183.63	82	183.63
Throughput (Mbps)	312	489.68	218.66	489.68
Efficiency (Mbps/Slices)	1.51	9.79	0.31	9.41

TABLE VII. PERFORMANCE COMPARISON OF PROPOSED WORK WITH EXISTING PHY TR IMPLEMENTATIONS [27 32]

Designs	PHY-TR	FPGA	Techniques	Slices	LUTs	Frequency (MHz)	Power (mW)
Mohandes et al. [27]	NB-PHY	Virtex-6	BCH	846	1293	60	162
Kizil et al. [28]	IR-UWB	Virtex-7	DWPT	557	3397	99	114
Jeong et al. [29]	HBC-PHY	Artix-7	FSDT	521	5231	32	114
Guruprasad and Chandrasekar [30]	PHY-TR	Artix-7	O-QPSK	224	1428	270	171
Sujaya and Bhanuprakash [31]	PHY-DTR	Artix-7	BCC	1646	2517	232	113
Sujaya and Bhanuprakash [32]	HBC-PHY	Artix-7	FSDT	196	1137	256	101
Proposed work	CSR-UWB	Artix-7	CSR	59	929	267.73	103

V. CONCLUSION AND FUTURE WORK

The CSR-UWB transceiver and its performance realization are discussed in this manuscript. The complete CSR-UWB transceiver is implemented on Artix-7 FPGA on the Xilinx environment at different code lengths. The CSR-UWB transmitter uses the shifting and reference codes to frame the transmitted data. In contrast, detection codes are used in the CSR-UWB receiver to recover the original input data information. An efficient autocorrelator and data detection unit are used at the receiver end to detect the original data without an additional synchronization mechanism. The CSR-UWB transceiver and its submodules are synthesized and realize the resource utilization after place and route operation. The CSR-UWB transceiver utilizes < 1 % slices and 1 % LUTs and operates at a frequency of 267.236 MHz on Artix-7 FPGA. The CSR-UWB transceiver achieves a throughput of 713.95 Mbps at code length eight. The proposed CSR-UWB transceiver is compared with existing CSR-UWB transceivers and different PHY transceiver designs with better improvement in performance metrics. The proposed CSR-UWB transceiver will be incorporated as a communication interface mechanism in IEEE 802.15.4a standards for wireless PAN applications to realize the performance constraint. The UWB transceiver is incorporated with MIMO based system to avoid the multipath effects and spatial diversity and also to improve the system accuracy.

COFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Conceptualization and Writing—review and editing: Santhosh Kumar R; Supervision: Rajashree N and Devaraju R; all authors had approved the final version.

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