Design of a High-Efficiency Doherty Power Amplifier for 5G Applications Using Wilkinson Power Divider

Issoufou G. Gremah Ary[1], George N. Kamucha[2], and Franklin Manene[3]
[1] Department of Electrical Engineering, Pan African University, Institute for Basic Sciences Technology and Innovation, PAUSTI, Nairobi-6200-00200, Kenya
[2] Department of Electrical and Information Engineering, University of Nairobi, Nairobi-00100, Kenya
[3] Department of Electrical and Control Engineering, Egerton University, Nakuru-20107, Kenya
Email: issoufougremah@gmail.com; gkamucha@uonbi.ac.ke; manenef@gmail.com

Abstract —In this paper, a novel Doherty Power Amplifier DPA based on a 10 W gallium-nitride high-electron-mobility transistor (GaN-HEMT) technology is designed using Advanced Design System (ADS) software. In the design, two different single Power Amplifiers (PAs) are combined using a Wilkinson power divider which is also used to connect the power to the load. The designed DPA operates in the range of 2.0-3.0 GHz and aims to achieve high efficiency, wide bandwidth and high output power for 5G applications. Simulation results showed a 40% fractional bandwidth and more than 44 dBm of saturated output power. In addition, the Power-Added Efficiency (PAE) and Drain-efficiency (Deff) are about 77% and 84%, respectively. A comparison with the other previous works shows enhancement in the maximum large-signal gain (L_S_Gain) in the average of 2.5 dB and an average PAE of about 10%. This improvement can be attributed to the deployment of the power divider/combiner proposed in the design and also the optimization of the components during the design.

Index Terms—Doherty power amplifier (DPA), GaN-HEMT, power divider/combiner, efficiency

I. Introduction

Radiofrequency (RF)/microwave components are widely used in communication systems such as satellite communications, radars, VSAT, point-to-point networks, and other wireless communications systems. One of the key components employed in these systems is the power amplifier (PA). The performance of the power amplifier used in any wireless system affects the system's overall performance [1]. The demand for high-performance transceivers has grown with the recent evolution of wireless systems. Today's wireless communication services have a high-speed demand that has led to the use of fifth-generation (5G) communication systems [2]. However, 5G communication uses complex modulations schemes such as Long Term Evolution (LTE), Orthogonal Frequency Division Multiplexing (OFDM), which have a high peak to average power ratio (PAPR) [3], [4]. However, high PAPR affects the performance of PA in a transmitter chain. Hence the PA in 5G systems must deliver excellent efficiency, gain, linearity, and output power across wider bandwidths. Since the PA is the most power-consuming element in a transceiver's system, it needs to be as efficient as possible.

Traditional power amplifiers used in communication systems have high efficiency only at saturation. Still, thanks to high PAPR in current modulations, the efficiency demonstrates a severe loss with output power backoff [5]. Different alternatives have been proposed to enhance efficiency at backoff, such as Envelope Tracking (ET) [6], Envelope Elimination and Restoration (EER) [7], and Doherty Power Amplifier (DPA). DPAs have been preferred because of their simple form and low cost.

A high amount of power consumption affects the communication industries, putting more pressure on financial and social aspects on them. With the still-growing demand for communication equipment, the energy demand is also increasing. With 80% of power consumption in wireless communication equipment, the RF power amplifier needs to be efficient to reduce its energy consumption [8]. In addition, the significance of Information and Communication Technology (ICT) in global greenhouse gas emissions is becoming increasingly crucial, as it is predicted to increase by 50% by the year 2030. Wireless communications, being a key component of ICT, are responsible for the main part of energy consumption [9], [10]. Therefore, the design of high-efficiency PAs is of utmost importance.

In this paper, a novel method where two PAs are designed and combined to form a DPA is proposed. The DPA works in the frequency range from 2.0 GHz to 3.0 GHz, achieving a high efficiency by considering other parameters such as bandwidth. Radiofrequency field-effect transistor model, CGH40010F GaN HEMT from Cree Wolfspeed Inc suppliers, was used for the design. The choice of this transistor was due to its advantage of high efficiency, high gain, and wide bandwidth. The transistor is also suitable for linear amplifiers with complex modulations which correspond to modulations used in 5G [11].

The rest of the paper is organized as follows. In Section II, the structures, the input and output matching of the DPA are presented, while in Section III, the simulation results of the DPA are presented and compared with those from literature. Finally, Section IV concludes the work.

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II. Doherty Power Amplifier

Named after its inventor W.H. Doherty in 1936, the Doherty power amplifier is one of the most common efficiency enhancement techniques [12]. The basic structure of the Doherty amplifier is shown in Fig. 1, where a power splitter divides the input RF signal effectively to the device gates. The devices consist mainly of the main and peaking amplifiers, biased in class AB and class C, respectively. A power combiner network is used to sum the signals to a load through an impedance transformer [13].

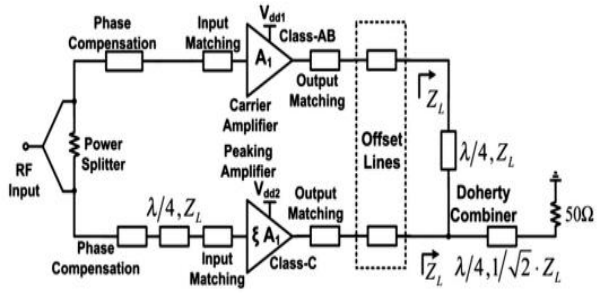


Fig. 1. Doherty power amplifier structure [13]

In evaluating the performance of a DPA, several parameters are considered, including output power, gain, linearity, and efficiency. The output power P_{out} of a DPA is the power delivered to the external load (usually 50Ω) in a frequency band of [f_{Low}, f_{High}], and is expressed as [14]:

$$P_{out} = P_{out(f)} = \frac{1}{2}\text{Re}\{V_{out}.I^*_{out}\}\ f \in [f_{Low}, f_{High}] \quad (1)$$

Output power is considered as the most important aspect of PA characteristic because it has a trade-off between power gain and efficiency.

Another parameter to consider while designing a DPA is the gain. It is defined as the ratio of output power to the input power and is expressed as:

$$G = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (2)$$

where G is the gain of an amplifier in dB, Pout and Pin are output power and input power in watt, respectively.

Another important parameter to evaluate DPA performance is efficiency. There are two categories of efficiency: Drain Efficiency (DE) and Power Added Efficiency (PAE). DE is defined as the ratio of RF output to DC power dissipation, as described in the equation below:

$$DE = \frac{P_{out}}{P_{DC}} \quad (3)$$

PAE demonstrates the ability of the PA to transform DC power to RF power. It is obtained as the difference between the RF output power, Pout, and the RF input power, Pin, to the DC power, P_{DC} given as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (4)$$

Linearity plays an important role in designing a DPA. It is described as a situation in which the device's output fluctuates linearly in response to changes in the input. In today's RF communication systems, linearity is becoming increasingly critical. In general, the linearity is determined by the third-order intercept point (IP3) value. The intercept point is determined by graphing the output power against the input power graph on a logarithmic scale. The output power acquired is linear to the input when the linearity is high.

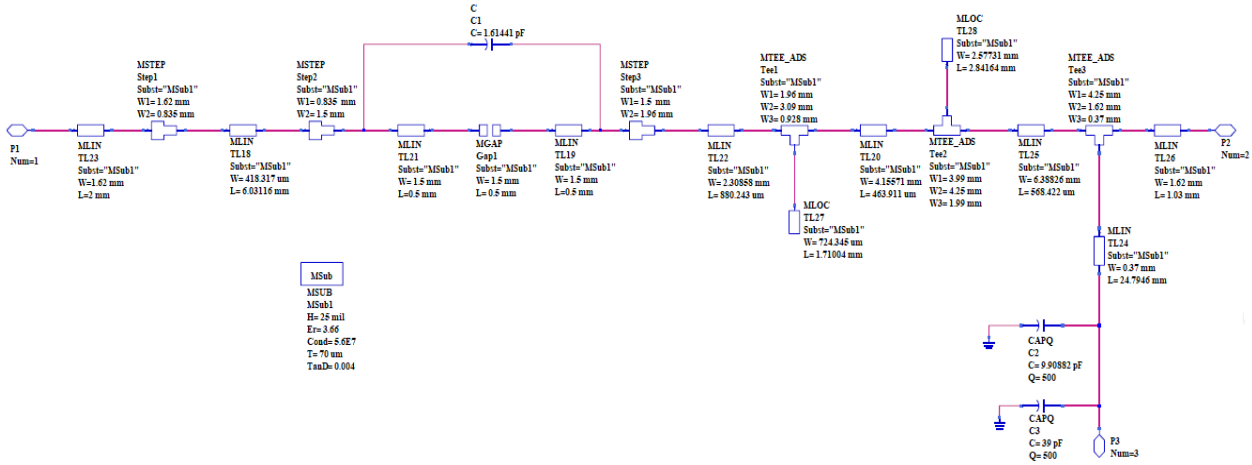
In [15] the authors presented a Doherty amplifier using a novel load–pull-based design technique and a new load modulation scheme to optimize the efficiency at the desired backoff level. Their simulation results showed good saturated output power and drain efficiency. But the design had a drawback of low PAPR of around 8.3 dB, and again it uses a 3-way asymmetric Doherty power amplifier which means more cost. B. Wang *et al*. [16] proposed a design of asymmetric DPA to extend the power backoff level and achieve high efficiency. The method they proposed had the advantages of achieving a high gain and output power. Unfortunately, the power backoff they achieved was around 7 dB which is low for modern communication systems, and the PAE is also low compared with many other methods. In [17], B. M. Hamouda et al. proposed a method to design a highly efficient power amplifier, where input matching and output matching were designed using resonant circuit broadband matching, based on equiripple approximation and multi-section quarter-wave transformer, respectively. Their proposed PA showed a simulation of up to 72% drain efficiency and small-signal gain exceeding 14 dB. Nevertheless, the method led has a fractional bandwidth of about 28.5%, which is insufficient. In order to overcome the drawbacks of conventional DPA, H. Xiong *et al*. [18] proposed a new method to improve backoff efficiency and bandwidth. The method consisted of designing an asymmetric Doherty power amplifier using symmetric devices. The measured results of the proposed PA exhibited 50.6%-57.3% drain efficiency at 6 dB power backoff. However, for a signal with more PAPR (7.5dB), the efficiency dropped to 45% with 39 dBm output power.

From the reviewed works above, it can be seen that most power amplifiers designs emphasize on either efficiency, backoff efficiency, or bandwidth aspects. However, current wireless communication systems require a power amplifier that has a trade-off between all these parameters.

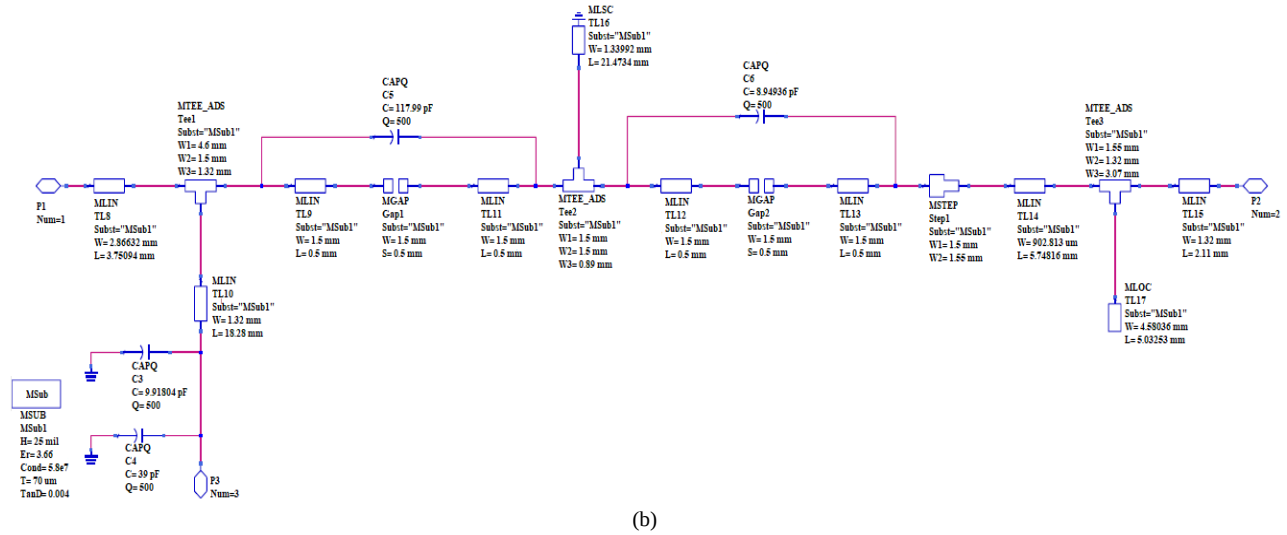
This paper proposes a novel Doherty power amplifier with a new power combiner network. Optimization techniques were also used to achieve high efficiency both at saturation and backoff power, better gain, and good bandwidth. Both design and simulations in this paper are done using advanced design system (ADS) software.

A. Design of the DPA Matching Networks

To design the DPA, first, a single PA is designed using a CGH40010F device. The CGH40010F from Cree is an unmatched gallium nitride (GaN) high electron mobility transistor (HEMT). It has a general-purpose broadband solution for a variety of RF and microwave applications that runs on a 28 V rail. As mentioned in its features, the design specifications to be achieved are 15 dB small-signal gain at 3.0 GHz, 41 dBm saturated output power and up to 65% efficiency at saturation [11]. The single PA comprises an input matching network, the transistor device, and an output matching network. There are many impedance matching techniques, such as transformer matching, lumped components matching, and transmission line matching while designing a matching network. The latter is used in this work, where both input and output matching networks are designed using microstrip transmission lines, as shown in Fig. 2. Therefore, ideal matching networks were designed first, then converted to microstrip matching networks. The ideal input matching network was designed using a smith chart, where a double step matching network was designed. For the ideal output matching network, an optimization method was used to perform the design and five ideal transmission lines, three series capacitors, and two steps were used.



(a)



(b)

Fig. 2. Matching networks design, (a) microstrip input matching network and (b) microstrip output matching network.

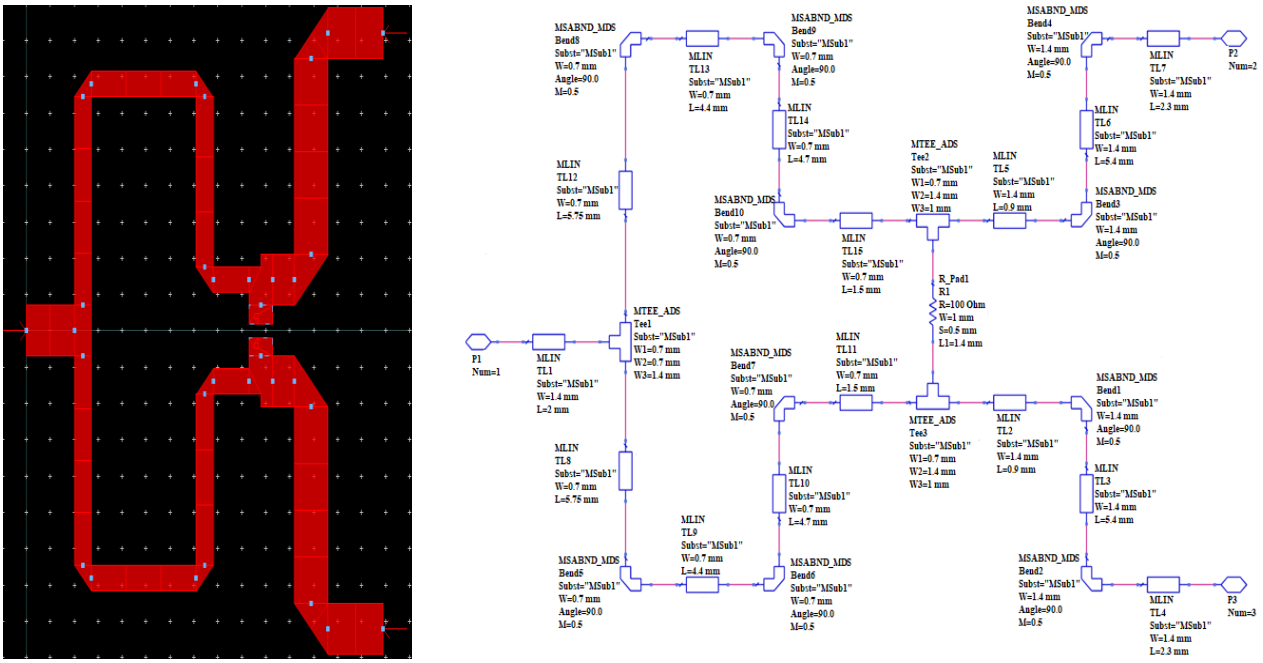
B. Design of Power Divider/Combiner

The input RF power needs to be shared with both the main and auxiliary amplifiers in a DPA. Therefore, a power divider is used for this task. The two amplifiers are combined to the load at the output level through a power combiner.

In this design, the same network divides the power at the input and combines it at the output. A layout design of the power divider/combiner is made first, then converted to a schematic, as illustrated in Fig. 3.

Printed circuit board (PCB) layout technology was used for the design, where a layer of 1.4 mm width and 2 mm length was used. The substrate used for the EM simulation is a FR_4_Prepreg (4.6) material with a dielectric constant E_r=3.66 and a thickness=0.762 mm. The simulation results of s-parameters using microstrip transmission lines shown in Fig. 4 achieve a reflection

coefficient S11 of less than -10 dB in the entire frequency band and a gain S21, S31 of around -3 dB.



(a) (b)

Fig. 3. Power divider/combiner design, (a) layout of the power divider/combiner, and (b) schematic of the power divider/combiner.

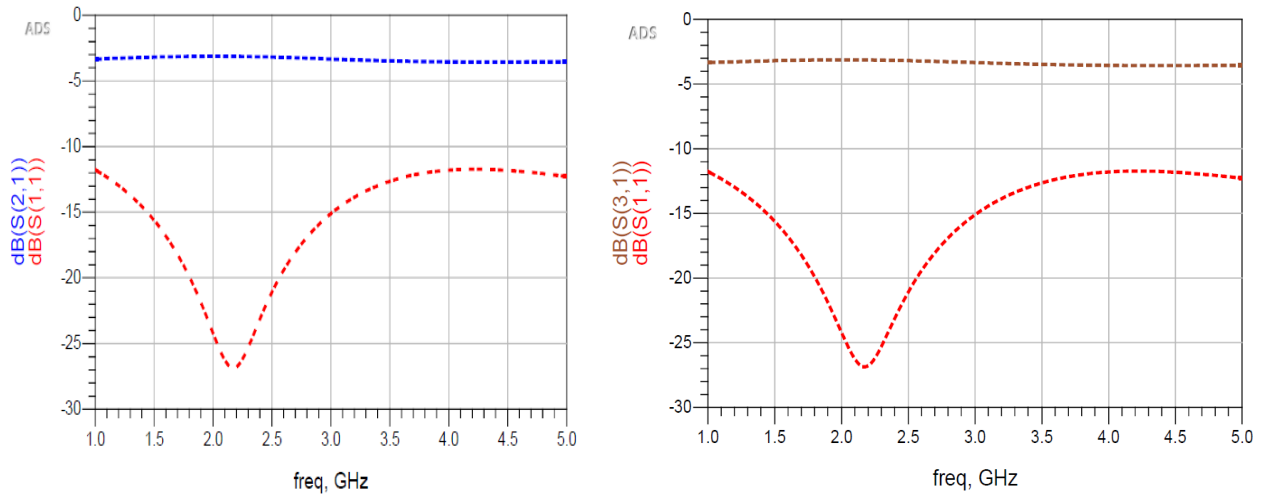


Fig. 4. S-Parameters simulations of the power divider/combiner

The designed power divider/combiner is a Wilkinson power divider. A power divider's three-port network is lossless when the output ports are matched, where only reflected power is dissipated [19]. Input power can be divided into two or more in-phase signals with the same amplitude.

In this design, the same network divides and combines the power. At the input side, the network works as a divider, where one port shares the power to two different ports, while at the output, it plays the role of the combiner, where two different ports are combined to form a single port.

III. Simulations Performance of the DPA

The designed DPA shown in Fig. 5 is implemented using microstrip transmission line components, where two identical devices, CGH40010F, were used. The main and auxiliary amplifiers are biased with the same supply voltage of 28V, and a gate voltage of -2.7 V. The microstrip substrate (MSub) used to design the complete DPA has a relative dielectric constant E_r=3.66, a substrate thickness H=0.625 mm, a conductor conductivity Cond=5.8e7, a conductor thickness T=70 um and a dielectric loss tangent TanD=0.004.

The simulation results of small-signal in Fig. 6 shows input and output return loss of better than -10 dB in the frequency range of 2.4 GHz to 2.6 GHz and less than -3 dB in the entire frequency band, while the gain is about 10 dB over the whole frequency band (2 GHz to 3 GHz).

The performance of the DPA in terms of large-signal-gain (LS_Gain), the power delivered (Pdel), drain efficiency (Deff), and power-added efficiency (PAE) are demonstrated in Figs. 7(a), 7(b) and 8, respectively.

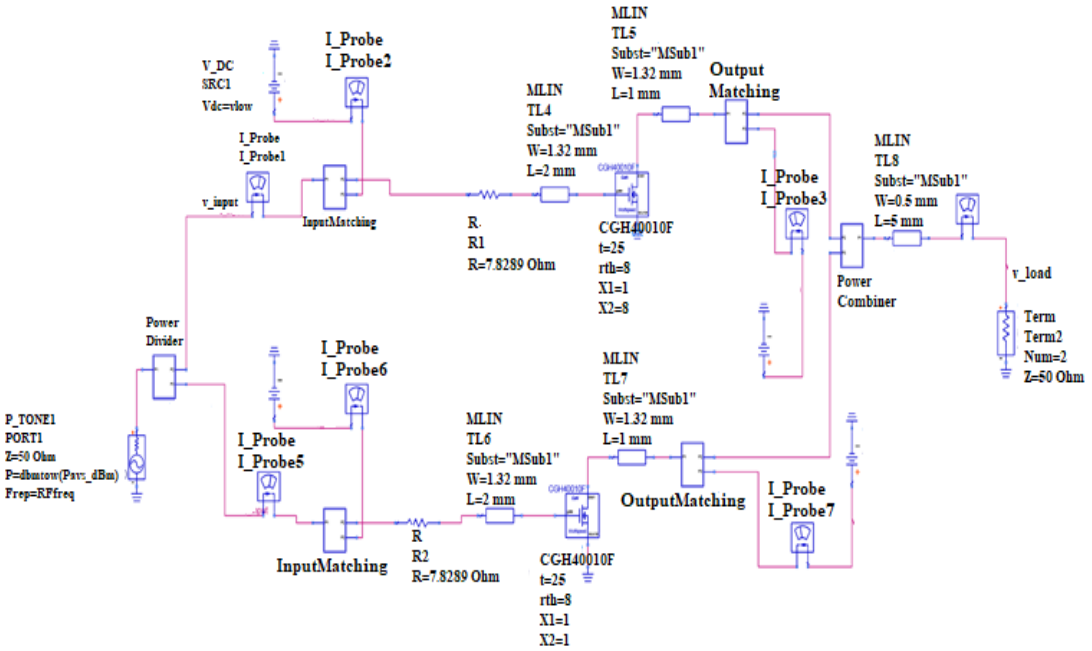


Fig. 5. DPA complete schematic.

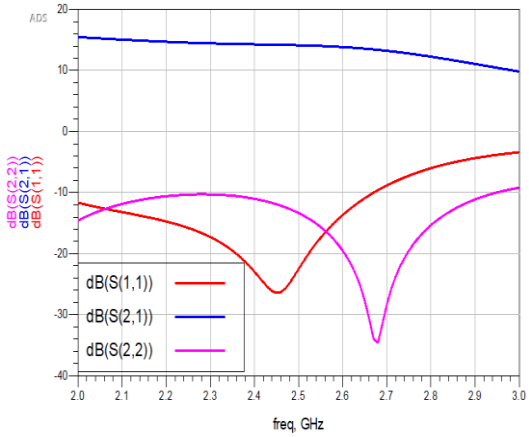
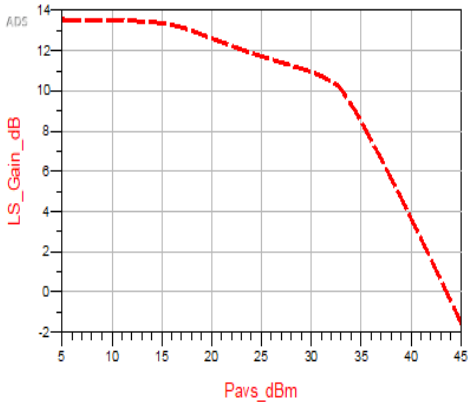
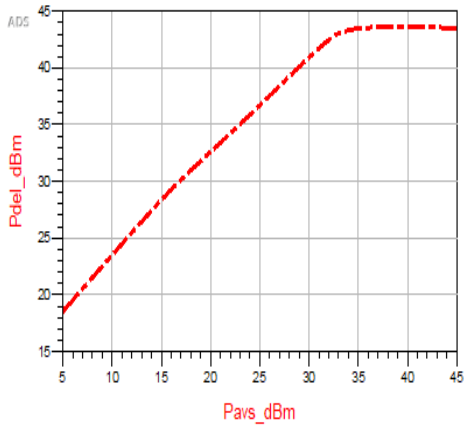


Fig. 6. S-parameters results of the DPA.

As illustrated in Fig. 7, the large-signal gain versus input power is plotted. The result shows a gain of about 14 dB at small input power; nevertheless, it drops to a low value with the input power increase due to gain compression. The output power versus input power is also shown in the same figure, where an output power of about 44 dBm is achieved at saturation.



(a)



(b)

Fig. 7. S- DPA performance, (a) gain plot, and (b) power delivered plot DPA.

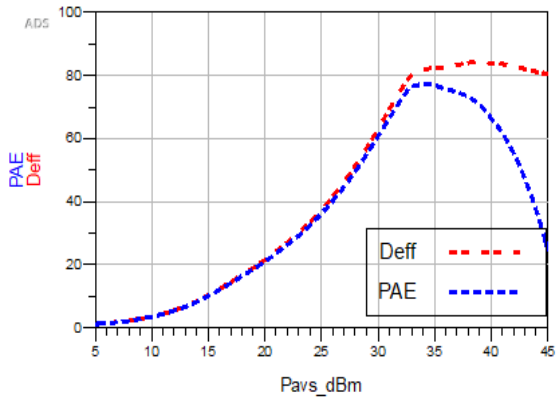


Fig. 8. DPA efficiencies.

Efficiency is another important parameter to evaluate DPA performance. As it can be seen from Fig. 8, the Deff and PAE of the designed amplifier are simulated, where about 84% and 77% of Deff and PAE are achieved at

saturation, respectively. In addition, the PAE at 9dB backoff is about 70%.

The fractional bandwidth of the designed DPA is also calculated. As stated in [20], the fractional bandwidth is defined as:

$$BW(\%) = \frac{\Delta f}{f_c} \quad (5)$$

where Δf is the absolute bandwidth and f_c the center frequency.

The arithmetic mean of the upper and lower frequencies is commonly used to define the center frequency, so that:

$$f_c = \frac{f_H + f_L}{2} \quad (6)$$

From these equations and figure 6, we can deduce the center and the fractional bandwidth of the designed DPA as follows:

$$f_c = \frac{2+3}{2} = 2.5GHz \quad (7)$$

$$BW(\%) = \frac{3-2}{2.5} * 100 = 40\% \quad (8)$$

The achieved simulation results of this study are compared to those of the previous study, as illustrated in Table I.

TABLE I: COMPARISON WITH THE OTHERS PREVIOUS WORKS

Ref.	Frequency (GHz)	P_{Out}sat (dBm)	OBO(dB)	PAE@OBO (%)	Gain (dB)
[21]	2.8-3.6	44	6	42%	10
[22]	3.3-3.5	48	8	54-64	10
[23]	3.4-3.8	48	13	50-60*	12.5
[24]	2.8-3.6	44.2	6	44-56*	13.5
This Work	2.0-3.0	44	9	25-70	14

*Drain efficiency@OBO
OBO: output backoff

IV. CONCLUSION

A Doherty power amplifier with a Wilkinson power divider and combiner using the 10 W GaN-HEMT technology have been presented. The designed amplifier worked in the 2.0-3.0 GHz frequency range and achieved a 9 dB backoff power. First, a simple PA was designed, then used to develop the DPA with a power divider and combiner at the input and load points. After that, the DPA was simulated, and results showed a reflections coefficient of less than -3dB in the whole frequency band, while Deff, PAE, output power and gain are about 84%, 77%, 44 dBm, and 14 dB, respectively. Finally, compared with other previous works, the designed DPA has better performance in gain and PAE.

In future, an implementation of this design can be considered. Also, linearity is not considered in this design. Digital Signal Processing (DSP) can be applied to improve the linearity of the design in future.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Issoufou Grah Gremah Ary conducted the research, performed the design and simulations of results, contributed reagents materials and wrote the manuscript. George Kamucha contributed to the design reagents and reviewed the results and the manuscript. Franklin Manene contributed to the design and adjusted the manuscript.

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REFERENCES

[1] K. Nakatani, Y. Yamaguchi, M. Hangai, and S. Shinjo, "A Ka-Band CW 15.5W 15.6% fractional bandwidth GaN Power amplifier MMIC using wideband BPF inter-stage matching network," *IEEE BiCMOS Compd. Semicond. Integr. Circuits Technol. Symp.*, pp. 50–53, 2019.

[2] K. Kaur, S. Kumar, and A. Baliyan, "5G: A new era of wireless communication," *Int. J. Inf. Technol.*, vol. 12, no. 2, pp. 619–624, 2020.

[3] S. Nagul, "A review on 5G modulation schemes and their comparisons for future wireless communications," in *Proc. Conf. Signal Process. Commun. Eng. Syst. SPACES 2018*, vol. 2018-Janua, 2018, pp. 72–76.

[4] R. Kumari, M. Chawla, and M. T. Scholar, "Review of PAPR reduction techniques for 5G system," vol. 10, no. 1, pp. 35–44, 2017.

[5] E. Bertran, "Assessment of the peak-to-average power ratio in different channel organization strategies," *Telecommun. Syst.*, vol. 62, no. 2, pp. 363–373, 2016.

[6] F. Wang, A. H. Yang, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4 I, pp. 1244–1254, 2005.

[7] F. Wang, *et al.*, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," in *Proc.IEEE MTT-S Int. Microw. Symp. Dig.*, May 2014, pp. 645–648.

[8] L. Liu, S. Men, M. Liu, and B. Zhou, "An energy saving solution for wireless," pp. 31–33, 2015.

[9] G. Y. Li, Z. Xu, C. Xiong, C. Yang, S. Zhang, Y. Chen, and S. Xu, "Energy-Efficient wireless communications: tutorial, survey, and open issues," *IEEE Wirel. Commun.*, vol. 2, no. 4, pp. 1–11, 2011.

[10] i-SCOOP. [Online]. Available: https://www.i-scoop.eu/

[11] Wolfspeed [Online]. Available: https://www.wolfspeed.com/cgh40010
[12] W. H. Doherty, "A new high - efficiency power amplifier for modulated waves," *Bell Syst. Tech. J.*, vol. 15, no. 3, pp. 469–475, 1936.
[13] M. Sajedin, I. T. E. Elfergani, J. Rodriguez, R. Abd-Alhameed, and M. F. Barciela, "A survey on RF and microwave doherty power amplifier for mobile handset applications," *Electron.*, vol. 8, no. 6, 2019.
[14] P. F. M. G. Prof. Abbas Mohammadi, *RF Transceiver Design for MIMO Wireless Communications*, vol. 145. 2012.
[15] J. Son, I. Kim, J. Moon, J. Lee, and B. Kim, "A highly efficient asymmetric doherty power amplifier with a new output combining circuit," in *Proc. IEEE Int. Conf. Microwaves, Commun. Antennas Electron. Syst. COMCAS 2011*, vol. 2, pp. 7–10, 2011.
[16] B. Wang, J. Teng, X. Zhang, D. Su, and W. Luo, "High-Efficiency doherty power amplifier based on an asymmetric structure," *Engieering World Open Access J.*, vol. 2, pp. 264–269, 2020.
[17] B. M. Hamouda, B. M. Abdelrahman, and H. N. Ahmed, "A 3.5-GHz, highly-efficient power amplifier for wireless communication applications," in *Proc. 12th Int. Conf. Electr. Eng. ICEENG 2020*, 2020, pp. 331–334.
[18] H. Xiong, W. Chen, L. Chen, X. Chen, and Z. Feng, "A High Efficiency Asymmetric Doherty Power Amplifier Using Symmetric Devices for 5G Application," in *Proc. Int. Conf. Microw. Millim. Wave Technol. ICMMT 2018 - Proc.*, 2018, pp. 1–3.
[19] F. S. Gomha and K. Langat, "Design and performance optimization of a wide band millimeter-wave power amplifier in 130 nm SiGe BiCMOS technology," vol. 12, no. 7, pp. 1053–1063, 2019.
[20] W. L. Stutzman and G. A. Theiele, *Antenna Theory and Design*, (2nd ed.). New York, 1998.
[21] A. Veshaj, A. Piacibello, C. Ramella, A. Nasri, V. Camarchia, and M. Pirola, "Design strategy of a 2.8-3.6 GHz 20W GaN Doherty power amplifier," in *Proc. Int. Work. Integr. Nonlinear Microw. Millimetre-Wave Circuits, INMMiC 2020 - Proc.*, 2020, pp. 4–6.
[22] A. M. Abdulkhaleq, *et al.*, "A 70-W asymmetrical doherty power amplifier for 5G base stations," *Lect. Notes Inst. Comput. Sci. Soc. Telecommun. Eng. LNICST*, vol. 263, pp. 446–454, 2019.
[23] A. M. Abdulkhaleq, *et al.*, "Three-way doherty power amplifier using class-f amplifier for more efficient mobile communications," *Pervasive Health Pervasive Comput. Technol. Healthc.*, vol. 2, no. 9, pp. 1439–1448, 2020.
[24] A. Nasri, *et al.*, "Design of a wideband doherty power amplifier with high efficiency for 5g application," *Electron.*, vol. 10, no. 8, pp. 1–13, 2021.

Issoufou G. Gremah Ary was born in Maine Soroa, Niger, in 1995. He received a B.Sc. degree in automation and industrial IT from the university institute of technology at Dan Dicko Dankoulodo University, Maradi, Niger, in 2019. He is currently an M.Sc student in electrical engineering (telecommunication-option) at Pan African University, Nairobi, Kenya. His current research includes microwave engineering and wireless communications systems.

George Kamucha received his PhD degree in Electrical Engineering from Kassel University, Germany, in 2003. He is currently a Senior Lecturer and Chairman of the Department of Electrical and Information Engineering, University of Nairobi, Kenya. His current research interests include communication and biomedical systems.

Franklin Manene is a lecturer in the Department of Electrical and Control Engineering, Egerton University Kenya. He received his Bachelor of Technology degree in Electrical communication engineering from Moi University (Kenya) in 1999. He obtained a Master of Science degree in Electrical engineering (Telecommunications engineering) from Jomo Kenyatta University of Agriculture and Technology, faculty of engineering, in 2007. He was awarded a PhD in Electrical Engineering (Electromagnetics) in 2014 from Florida Institute of Technology, USA.