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High-Performance and Low-Complexity Decoding Algorithms for 5G Low-Density Parity-Check Codes

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Abstract —The development of the Fifth Generation (5G) New Radio (NR) provides several significant advantages when compared to the fourth generation (4G) Long Term Evolution (LTE) in mobile communications. Due to the outstanding characteristics of Low-Density Parity-Check (LDPC) codes such as high decoding performance, high throughput, low complexity, they have been accepted as the standard codes for the 5G NR. In this paper, we propose two LDPC decoding algorithms: Hybrid Offset Min-Sum (HOMS) and Variable Offset Min-Sum (VOMS), which are aimed at improving the error correction performance. The main idea of the HOMS/VOMS algorithm is to apply modified factors to both variable-nodes and check-nodes updated processing in order to compensate the extrinsic messages overestimation of the MS-based algorithms and increase the protection ability for degree-1 variable-nodes. The simulation results show that at the Bit-Error-Rate (BER) of 10^{-5}, the proposed HOMS/VOMS algorithm achieves the decoding gain up to 0.2 dB compared to the Offset Min-Sum (OMS) algorithm, with a slight increase in decoding complexity.

Index Terms—LDPC codes, 5G New Radio, Belief propagation, Min-Sum decoding, Offset Min-Sum decoding

I. Introduction

Low-Density Parity-Check (LDPC) codes, presented by Robert Gallager in 1962, provide near-capacity performance [1]. In the last decades, LDPC codes have been received increasing attention because of their excellent performance. They are among the most widely used types of Forward Error Correction (FEC) codes in various aspects of communications standards such as Digital Video Broadcast (DVB) [2], wireless standards including IEEE 802.11 [3], and Advanced Television System Committee (ATSC) [4]. Especially, LDPC codes have been accepted by Third Generation Partnership Project (3GPP) as the standard codes for the enhanced Mobile Broadband (eMBB) data channel of the 5G mobile communications [5], [6].

LDPC codes are generally decoded by an iterative message-passing algorithm. The main idea of these algorithms is that Variable-Nodes (VN) and check-nodes (CN) can exchange messages with each other during each iteration processing. The typical decoding algorithm is known as the Belief-Propagation (BP) algorithm [7]. The BP algorithm achieves the decoding performance very close to the Shannon limit [8], to the detriment of computational complexity and hardware implementation [9]. To overcome these disadvantages, the Min-Sum (MS) algorithm [10] was proposed by using max-log approximation of the check-node processing. The only computations required by the MS decoding are additions and comparisons, which solves the complexity significantly. Despite the low complexity is achieved, the minimum function in CN processing side generates an approximate message. This causes an overestimation of check-node messages, which leads to a degradation in the error-rate performance of the decoder. For this reason, many various modifications of the original MS algorithm were proposed such as the Offset Min-Sum (OMS) [11] and the Normalized Min-Sum (NMS) [12]. In these modified algorithms, a normalization or an offset factor is directly applied to the CN-update function of the original MS algorithm in order to compensate the overestimation of check-to-variable messages. However, the performance gap between the BP and the existing MS-based decoding algorithms still gives room for further improvement in terms of the decoding performance.

In [13], Two-Dimensional (2-D) correction schemes were proposed for irregular LDPC codes, which searched the normalization factor pair (α,β) applying for each variable and check-node units. These factors depended on the degree of the corresponding nodes. The optimal normalization factor pair (α,β) were obtained by using an iterative procedure. This process is based on parallel differential optimization. In terms of design complexity, these proposed algorithms required extra memory for storing the normalization factors. Moreover, they needed more computational complexity to choose a different factor for each degree. Another modification of the MS algorithm was the Variable Global Optimization Min-Sum (VGOMS) algorithm [14]. It used the optimization scaling factor multiplied in the variable-node operation. To obtain the improved error correction performance, the Particle Swarm Optimization (PSO) technique was applied to determine the value of the optimal scaling factor. This leads to an increase in the complexity of the variable node implementation. The single-minimum MS algorithm (smMS) was presented first in [15], in which a

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weight factor was added to the minimum value instead of calculating the second minimum. This approach is simple but has a high error floor. The improved version of the smMS was a variable weight smMS in [16], in which the correction factors depended on the iteration number. This algorithm gives significantly better error correction performance and reduces the decoder complexity. In [17], the Improved Offset Min-Sum (IOMS) decoder was proposed in order to improve the error correction performance. The idea of the IOMS algorithm is based on the OMS algorithm by adding multiplication factors to modify the check-node updating. These optimal factors were obtained by combining the Density Evolution (DE) [18] and simulation methods. The IOMS improved its performance with an acceptable increase in decoding complexity.

This paper proposes two algorithms HOMS and VOMS aimed at improving the 5G LDPC decoder's error correction performance. These proposals are originated from the following key causes:

- Firstly, due to the special properties of 5G LDPC codes, there are a lot of degree-1 VNs in extension columns of base matrix, which only connected to a unique CN. Thus, the reliability of check-to-variable message has a substantial influence on these VNs. These VNs are weakly protected and very sensitive to be erroneous. As a result, they significantly affect the decoding performance. Therefore, in order to reduce the error probability of degree-1 VNs and improve the error correction capacity, the VNs and/or CNs updated processing can be affected by using the appropriate correction factors.
- Secondly, from the state-of-the-art implementations, the error correction performance can be further improved based on OMS algorithm.

Inspired by important characteristics above, it can be observed that 5G LDPC decoding performance can be improved by applying the modified factors to the VNs and/or CNs updated processing. Simulation results show that two proposed algorithms HOMS and VOMS achieve an enhancement decoding performance, with only slightly increasing decoding complexity compared to the existing MS-based algorithms.

The remainder of this paper is organized as follows. In Section II, the basics of 5G LDPC codes and the proposed decoding algorithms HOMS and VOMS are described in detail. Section III exhibits the simulation results. The computational complexity of the LDPC decoder is analyzed in Section IV. Finally, Section V concludes the paper.

II. Preliminaries

A. 5G LDPC Codes

The LDPC codes with the length of the codeword length N and information block length K can be presented by a sparse parity-check matrix H with M rows and N columns where $M = N - K$. The code rate is denoted by R and $R = K / N$. Each row of H corresponds to a check-node (CN), while each column corresponds to a variable-node (VN). Besides, the LDPC codes can be represented graphically using a bipartite Tanner graph [19], in which each VN represents a code symbol, and each CN represents a parity equation. An edge connects a VN i and a CN j if and only if $H(j,i) = 1$ $(i = 1, \ldots, N; j = 1, \ldots, M)$. The number of 1's in a column or row is called its degree. This bipartite graph representation is very useful for describing the message-passing decoding algorithms.

In this work, a codeword $c = (c_1, c_2, \ldots, c_N)$ of the LDPC code is transmitted using the Binary Phase-Shift Keying (BPSK) modulation, which maps the coded bits into a transmitted sequence $x = (x_1, x_2, \ldots, x_N)$, according to $x_n = 1 - c_n$, $n \in [1, N]$. The transmitted codeword x is affected by noise transmitted through the channel. We consider a codeword x that is sent over an Additive White Gaussian Noise (AWGN) channel model. The output of the channel can be described by $y_n = x_n + z_n$; where z_n is an independent Gaussian random variable with zero mean and variance $\sigma^2 = N_0/2$. An LDPC can correct the transmitted codes by using Message-Passing (MP) iterative algorithm. The main idea of this method is to exchange messages between CNs and VNs iteratively. This process is implemented repeatedly until a codeword has been found (i.e., it satisfies all the syndromes check equations), or if the maximum number of iterations has been reached.

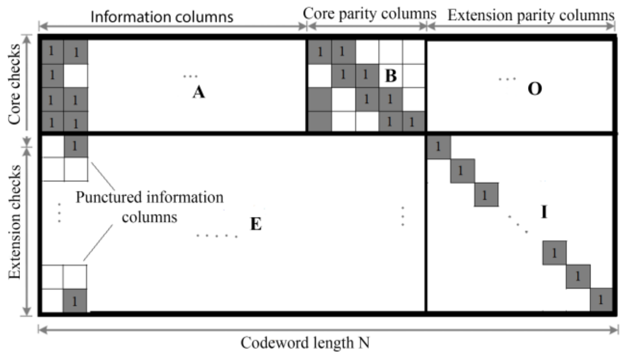

Fig. 1. Base matrix structure for the 5G QC-LDPC codes [22].

One of the classes of structured LDPC codes is Quasi-Cyclic LDPC (QC-LDPC), which widely used in practical applications [20]. As a special kind of structured code, QC-LDPC has the rate-compatible property and can support multiple lifting sizes. These properties make this code easily adapt various information lengths and rate matching [21], [22]. QC-LDPC codes are generally specified as a base matrix B of size $L\times C$ with entries $b_{i,j} \geq -1 \left(i \in \{1, 2, \cdots, L\}; j \in \{1, 2, \cdots, C\} \right)$.

The parity-check matrix H of a QC-LDPC code can be defined by expanding its base graph by an expansion factor Z. Thus, each entry in the base graph is replaced by a sparse matrix of size $Z\times Z$, defined as follows: entries $b_{i,j} = -1$ are replaced by the all-zero matrix and entries $b_{i,j} > -1$ are replaced by a circulant permutation matrix, obtained by right shifting the identity matrix by $b_{i,j} > -1$

positions. 5G LDPC codes use a quasi-cyclic structure, where the parity-check matrix (PCM) is defined by a smaller that enables low coding complexity. Fig. 1 shows the general structure of the base matrix for 5G LDPC codes. It can be observed that the base matrix consists of mainly five parts. Consider the matrix row-by-row side, we can see that the rows of the base matrix are divided into two parts: extension check rows and core check rows. The submatrix A corresponds to systematic bits. The submatrix B corresponds to the first set of parity bits. It is a square matrix with a dual-diagonal structure: its first column is of weight 3, whereas the submatrix composed of other columns after the first column has an upper dual-diagonal structure. Submatrix I is an identity matrix, and submatrix O is an all-zero matrix. The combination of A and B is referred to as the core checks, and the other parts (O, E, and I) are referred to as the extension checks. Similarly, consider the matrix column-by-column side, it can be observed that the columns of the base matrix are divided into three parts: information columns, core parity columns, and extension parity columns.

Accordingly, 3GPP has agreed to consider two QC-LDPC base-matrices named BGl and BG2 with similar structures illustrated in Fig. 1, a 1 in the matrix indicates the existence of a base edge. The BG1 is targeted for larger information block lengths ($500 \le K \le 8448$) and higher rates ($1/3 \le R \le 8/9$), while BG2 is targeted for smaller information block lengths ($40 \le K \le 2560$) and lower rates ($1/5 \le R \le 2/3$). In this paper, base graph BG1, the main 5G high-rate base graph is represented. BG1 has 22 information bit columns. Thus, any information block length is $22.Z$ where Z is called as the expansion factor. One of the special features in the 5G LDPC codes is the punctured variable-nodes. In the BG1, the leftmost two columns correspond to the $22.Z$ state bits, which are punctured before transmission. Its advantages are an improvement of performance at lower complexity and an effect on the number of base CNs. For BG1, the size of the parity-check matrix H generated is $46Z \times 68Z$. It is also worth noting that, the 5G LDPC codes are irregular. That means the check-node degree (d_c) and variable-node degree (d_v) vary significantly. In BG1 of the 5G LDPC codes, d_c varies from 3 to 19 and d_v varies from 1 to 30 [23].

B. Proposed Algorithms

In this section, to make a further improvement of the error correction performance based on the OMS algorithm, two modified algorithms are proposed. As mentioned above, the LDPC decoder will stop when all the check equations are satisfied (i.e., all the syndromes check equations equal to zero). However, in practice, some check-nodes might be checked in error. In that case, there may have at least one variable-node which transforms the wrong message to this check-node. By the rule of message-passing algorithms, the messages updated at this check-node are not reliable and unexpected. Based on these observations, in this work, we focus on considering the improvements in error correction characteristics at check-nodes and/or variable-nodes. We discuss in more detail as below.

The following notations concern the iterative decoding of LDPC codes reflecting in the exchange of information between the VNs and CNs and will be used throughout the paper:

- $H(n)$ is the set of check-nodes connected to the variable-node n, also referred to as the set of neighbor check-nodes of n.
- $H(m)$ is the set of variable-nodes connected to the check-node m, also referred to as the set of neighbor variable-nodes of m.
- $H(n)\backslash m$ is the set $H(n)$ with check-node m excluded.
- $H(m)\backslash n$ is the set $H(m)$ with variable-node n excluded.
- γ_n is the priori information of the decoder concerning variable-node n.
- $\alpha_{m,n}$ is the message sent from variable-node n to check-node m.
- $\beta_{m,n}$ is the message sent from check-node m to variable-node n.
- $\tilde{\gamma}_n$ is the posteriori information provided by the decoder, concerning variable node n.

The conventional OMS [11] and the proposed HOMS, VOMS decoding algorithms are described in detail as follows.

Conventional OMS algorithm

Step 1. Initialization:

$$\gamma_n = \log \frac{\Pr(x_n = 0 \mid y_n)}{\Pr(x_n = 1 \mid y_n)} \tag{1}$$

A priori information:

$$\alpha_{m,n} = \gamma_n \tag{2}$$

Iteration process:

Step 2. CN-processing (Check-node processing):

$$\beta_{m,n} = \left(\prod_{n' \in H(m) \setminus n} sgn(\alpha_{m,n'}) \right) \cdot \max \left\{ \left(\min_{n' \in H(m) \setminus n} |\alpha_{m,n'}| \right) - \beta, 0 \right\} \tag{3}$$

where $\beta > 0$: the offset factor.

Step 3. VN-processing (Variable-node processing):

$$\alpha_{m,n} = \gamma_n + \sum_{m' \in H(n) \setminus m} \beta_{m',n} \tag{4}$$

Step 4. AP-update (a posteriori information update):

$$\tilde{\gamma}_n = \gamma_n + \sum_{m \in H(n)} \beta_{m,n} \tag{5}$$

Step 5. Hard decision:

$$\hat{x} = \frac{1 - sgn(\tilde{\gamma}_n)}{2} \tag{6}$$

At the end of each iteration, the decoder computes the syndrome check vector

$$s = H\hat{x}^T \quad (7)$$

where $\hat{x}$ is the estimation of the transmitted codeword.

The decoder will stop the decoding process if a codeword has been found (i.e., $s = 0$), or the maximum number of iterations has been reached.

First proposal: HOMS algorithm

As can be seen above, the OMS decoding compensates the overestimation for all check-node messages of MS decoding by introducing an offset factor $\beta > 0$ within the CN-processing step. This might lead to the fact that the decoding performance is generally reduced due to the influence of degree-1 VNs. To improve error correction performance, the proposed HOMS algorithm compensates the overestimation for both the check-node and variable-node operations. For the HOMS, the check-node processing is modified as following:

$$\beta_{m,n} = \begin{cases} \left(\prod_{n' \in H(m)\setminus n} sgn(\alpha_{m,n'})\right) \cdot \min_{n \in H(m)} |\alpha_{m,n}| & \text{if } |\alpha_{m,n}| = \min_{n \in H(m)} |\alpha_{m,n}| \\ \left(\prod_{n' \in H(m)\setminus n} sgn(\alpha_{m,n'})\right) \cdot \max\left\{\left(\min_{n \in H(m)} |\alpha_{m,n}|\right) - \beta, 0\right\} & \text{otherwise} \end{cases} \quad (8)$$

and variable-node processing (4) in Step 3 is modified as:

$$\alpha_{m,n} = \gamma_n + sgn\left(\sum_{m' \in H(n)\setminus m} \beta_{m',n}\right) \cdot \max\left(\sum_{m' \in H(n)\setminus m} \beta_{m',n} - \delta, 0\right) \quad (9)$$

where $\delta > 0$: the offset factor.

It can be observed that in the HOMS algorithm, the check-to-variable messages updating seems to be a combination of the MS and OMS algorithms. From a hardware design perspective, the message sent from check-node m to variable-node n (i.e., $\beta_{m,n}$), as shown in (3), can be found through the two first minimum values (called as *min1* and *min2*, respectively) and the index of the smallest value among the messages sent from the set of variable-nodes connected to the check-node m. For the HOMS algorithm, we propose that the check-to-variable messages are calculated via only the first minimum value, together with its index, and the maximum value between the *min1* − β and 0 as shown in (8). Although the HOMS algorithm requires an additional comparison and one subtraction, the hardware used to execute the check-node unit is still smaller than that of the conventional OMS algorithm. In order to compensate the extrinsic messages estimation, we propose to apply an offset factor to the variable-to-check messages as shown in (9). Compared to the original OMS algorithm, two steps CN-processing and VN-processing are new.

Second proposal: VOMS algorithm

The Variable Offset Min-Sum (VOMS) algorithm is almost the same as the OMS algorithm except for the variable-node processing step. For the VOMS, the variable-to-check messages updating can be described as following:

$$\alpha_{m,n} = \gamma_n + \tau \cdot \sum_{m' \in H(n)\setminus m} \beta_{m',n} \quad (10)$$

where $\tau > 0$: the normalization factor.

The optimization factor pairs (β,δ) (for the HOMS algorithm) and (β,τ) (for the VOMS algorithm) are obtained by combining the Density Evolution (DE) [19] and simulation methods. In this work, we show the optimal factors for 5G LDPC codes with the codeword lengths of 4080 and 13056, the target Bit-Error-Rate (BER) of 10^{-5}. The procedure to find the optimal factor pairs is discussed in detail as follows. First, δ (for the HOMS algorithm) or τ (for the VOMS algorithm) is fixed to 1, β is optimized by using DE. At the end of this step, the optimal β value is 0.4. Next, β is fixed to its optimal value (i.e., 0.4 in this case study), the optimization of τ or δ parameter is performed through simulation. The values of τ and δ are optimized such that the decoders achieve the error correction capacity is as close to the BP decoder as possible. Finally, the optimal τ or δ value is fixed, the optimization of β value is found again by simulation. Table I shows the optimal factors for the HOMS/VOMS at the target BER of 10^{-5}.

TABLE I: THE OPTIMAL FACTORS OBTAINED FOR 5G LDPC CODES WITH DIFFERENT CODEWORD LENGTHS

Algorithm/Codeword lengths	Value
HOMS [This work]/4080	(β, δ) = (0.4,0.375)
HOMS [This work]/13056	(β, δ) = (0.4,0.3)
VOMS [This work]/4080	(β, τ) = (0.4,0.92)
VOMS [This work]/13056	(β, τ) = (0.4,0.875)
IOMS [17]/4080	(η, γ) = (0.4, 0.92)
IOMS [17]/13056	(η, γ) = (0.4, 0.95)
OMS [11]/4080 and 13056	β = 0.4

III. SIMULATION RESULTS

In this section, we conduct Monte Carlo simulations for the 5G LDPC codes. The base matrix BG1 with code rates 1/2, 3/4 and 2/3 is considered. The codeword lengths N are 4080 and 13056 corresponding to the expansion factor Z of 60 and 192. The maximum number of decoding iterations is set to 20. The decoding performances of the HOMS and VOMS decoders are illustrated and compared with the OMS, IOMS, and BP decoders.

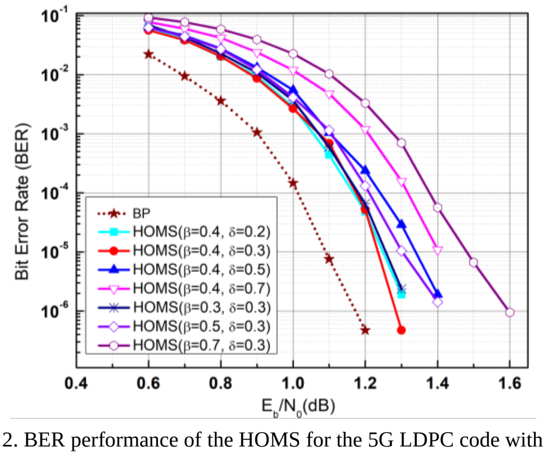

Fig. 2. BER performance of the HOMS for the 5G LDPC code with N = *13056; R = 1/2*, and the iteration number of *20*.

Fig. 2 depicts the error correction performance of the HOMS decoding algorithm with different values of the parameters β, δ and the BP algorithm.

The 5G LDPC code is considered with the codeword length N = 13056, and code rate of 0.5. The simulation results show that both β and δ factors have a significant effect on the BER. For instance, with $\beta = 0.4$ and $\delta = 0.3$, it can be seen that the HOMS algorithm gives the best error correction (i.e., BER curve is closer to BP) compared to the other ones.

For comparison purposes, we also include the BER performance of the OMS, IOMS and BP decoders as shown in Fig. 3. In this simulation, the 5G LDPC code with the codeword lengths N = 4080 and N = 13056, code rate $R = 3/4$ is considered.

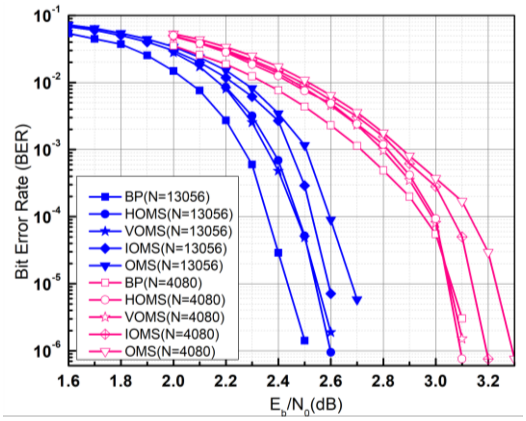

Fig. 3. Bit-error-rate (BER) performance of different decoding algorithms for 5G LDPC decoder with distinct codeword lengths N = *4080* and N = *13056*, code rate R = *3/4*, iteration number of *20*.

It is worth noting that at the target BER of 10^{-5}, the HOMS and VOMS algorithms have similar performance, and improve the decoding gain up to 0.2 dB compared to the OMS decoding. For the codeword length of 4080, they provide a decoding performance slightly better than the BP, while lower than the BP only by 0.1 dB in the case of codeword length N = 13056.

To further verify the performance of the HOMS/VOMS decoder, we simulate the 5G LDPC code with the codeword length of 13056, different code rates 1/2, 2/3 and 3/4 as shown in Fig. 4.

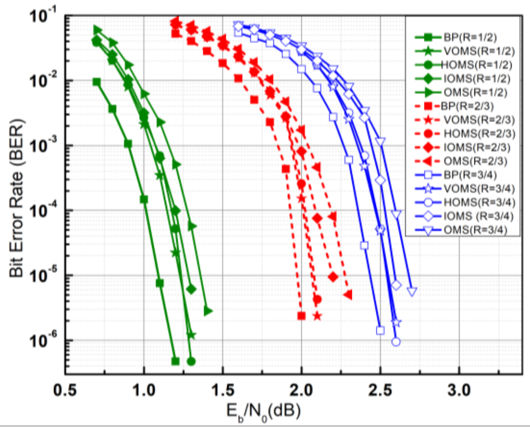

Fig. 4. BER performance for 5G LDPC codes with codeword length N = *13056*, iteration number of 20, the expansion factor Z = *192* and different code rates *1/2*, *2/3* and *3/4*.

It can be observed that the HOMS or VOMS decoder achieves the decoding gain close to the BP decoder (gap of 0.1 dB). Both HOMS and VOMS algorithms have almost the same decoding performance for all three code rates. In addition, they obtain the decoding gain of nearly 0.9 dB and 0.5 dB as the code rates vary from 1/2 to 2/3 and 2/3 to 3/4, respectively.

IV. Computational Complexity

In this section, we discuss about computational complexity of the check-node and variable-node units for some decoding algorithms. Table II shows the computational complexity of one check-node unit for the six decoders BP, MS, OMS, IOMS, VOMS and HOMS. The column 4 shows the required number of comparisons to find the first two minimum values using the XS approach [24].

TABLE II: The Check-Node Computational Complexity of Various Algorithms

Algorithm	Multiplications	Subtractions	Comparisons
BP	d_c	0	0
MS	0	0	$d_c - 2 + \lceil \log_2 d_c \rceil$
OMS	0	2	$d_c - 2 + \lceil \log_2 d_c \rceil$
HOMS	0	1	d_c
VOMS	0	2	$d_c - 2 + \lceil \log_2 d_c \rceil$
IOMS	0	2	$d_c - 2 + \lceil \log_2 d_c \rceil$

$\lceil x \rceil$ means x is mapped to the least integer greater than or equal to x.

As mentioned above, for the HOMS, finding only the first minimum value (*min1*) and its index greatly reduces the number of comparisons compared to other algorithms. Therefore, it can be observed that the HOMS requires the least number of comparisons among the other decoders except for the BP decoder. The VOMS, OMS, and IOMS need the same number of subtractions and comparisons, but the IOMS requires 2 multiplications for the normalized factor in one CN updating. The BP requires d_c multiplications but has no other operations.

Finally, the computational complexity for one variable-node unit (VN) processing for different decoders is given in Table III.

TABLE III: The Variable-Node Complexity Analysis of Various Decoders

Algorithm	Multiplications	Additions
BP	0	$d_v - 1$
MS	0	$d_v - 1$
OMS	0	$d_v - 1$
HOMS	0	d_v
VOMS	1	$d_v - 1$
IOMS	0	$d_v - 1$

Since the normalized or the offset factor is needed to implement the proposed VN-update function (as given by (9) and (10)), the HOMS or VOMS has a higher complexity than the others. However, this additional complexity is acceptable considering their improved error correction performance compared to the remaining decoders.

V. Summary

In this paper, two decoding algorithms HOMS and VOMS for 5G LDPC codes were presented. We aim to provide more decoding algorithm options and compare them with the existing decoders in terms of decoding performance and computational complexity. For the HOMS algorithm, both check-nodes and variable-nodes processing units are adjusted by applying the offset factor pair (β, δ). For the VOMS algorithm, the computational operation in the check-nodes processing is preserved (i.e., keep the same as OMS algorithm), while the variable-nodes processing is modified by applying the normalization factor τ to check-to-variable messages. The simulation results indicated that the HOMS and VOMS achieved decoding gain up to 0.2 dB compared to the existing MS-based decoding algorithms with an acceptable increase in decoding complexity.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Bich Ngoc Tran-Thi conceived the study, performed simulations, analyzed the results, wrote the manuscript. Both Thien Truong Nguyen-Ly and Trang Hoang supervised the project and contributed to the revision of the manuscript. All authors had approved the final version.

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References

[1] R. Gallager, "Low-density parity-check codes," *IRE Transactions on Information Theory*, vol. 8, no. 1, pp. 21-28, 1962.

[2] ETSI. ETSI EN 302 307 v1.3.1 Digital video broadcasting (DVB); second generation. (2013). [Online]. p. 2013-03. Available: https://www.dvb.org/standards/dvb-s2

[3] A. Balatsoukas-Stimming, N. Preyss, A. Cevrero, A. Burg, and C. Roth, "A parallelized layered QC-LDPC decoder for IEEE 802.11 ad," in *Proc. IEEE 11th International New Circuits and Systems Conference (NEWCAS)*, Paris, France, 2013, pp. 1-4.

[4] S. Myung, S. I. Park, K. J. Kim, J. Y. Lee, S. Kwon, and J. Kim, "Offset and normalized min-sum algorithms for ATSC 3.0 LDPC decoder," *IEEE Transactions on Broadcasting*, vol. 63, no 4, pp. 734-739, 2017.

[5] 3GPP. (2018). ETSI TS 138 212 V15.2.0 (2018-07) 5G NR Multiplexing and channel coding. (3GPP TS 38.212 version 15.2.0 Release 15), ETSI [Online]. Available: https://www.etsi.org/deliver/etsi_ts/138200_138299/138212/15.02.00_60/ts_138212v150200p.pdf

[6] Wf on LDPC parity check matrices, document Rl-1711982. 3GPP TSG RAN WG1 NR AH 2. (2017). [Online]. Available: https://www.3gpp.org/ftp/TSG_RAN/WG1_RL1/TSGR1_AH/NR_AH_1706/Docs

[7] T. J. Richardson and R. L. Urbanke, "The capacity of low-density parity-check codes under message-passing decoding," *IEEE Transactions on Information Theory*, vol 47, no 2, pp. 599-618, 2001.

[8] S. Y. Chung, G. D. Forney, T. J. Richardson, and R. Urbanke, "On the design of low-density parity-check codes within 0.0045 dB of the Shannon limit," *IEEE Communications Letters*, vol. 5, no. 2, pp. 58-60, 2001.

[9] Y. Kou, S. Lin, and M. P. C. Fossorier, "Low-density parity-check codes based on finite geometries: A rediscovery and new results," *IEEE Transactions on Information Theory*, vol. 47, no. 7, pp. 2711-2736, 2001.

[10] M. P. C. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," *IEEE Transactions on Communications*, vol. 47, no. 5, pp. 673-680, 1999.

[11] J. Chen, A. Dholakia, E. Eleftheriou, M. P. C. Fossorier, and X. Y. Hu, "Reduced-complexity decoding of LDPC codes," *IEEE Transactions on Communications*, vol. 53, no. 8, pp. 1288-1299, 2005.

[12] J. Chen, A. Dholakia, E. Eleftheriou, M. Fossorier, and X. Y. Hu, "Near optimal reduced-complexity decoding algorithms for LDPC codes," in *Proc. IEEE International Symposium on Information Theory*, Lausanne, Switzerland. 2002, p. 455.

[13] J. Zhang, M. Fossorier, D. Gu, and J. Zhang, "Two-dimensional correction for min-sum decoding of irregular LDPC codes," *IEEE Communications Letters*, vol. 10, no. 3, pp. 180–182, 2006.

[14] J. Suud, H. Zen, A. K. Othman, and K. A. Hamid, "Variable Global Optimization Min-Sum (VGOMS) algorithm of decode-and-forward protocol for the relay node in the cooperative channel," *Wireless Networks*, vol. 26, pp. 531–541, 2020.

[15] A. Darabiha, A. C. Carusone, and F. R. Kschischang, "A bit-serial approximate min-sum LDPC decoder and FPGA implementation," in *Proc. IEEE International Symposium on Circuits and Systems*, Kos, Greece, May 2006.

[16] C. Zhang, Z. Wang, J. Sha, L. Li, and J. Lin, "Flexible LDPC decoder design for multigigabit-per-second applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 1, pp. 116-124, 2010.

[17] B. N. Tran-Thi, T. T. Nguyen-Ly, H. N. Hong, and T. Hoang, "An improved offset min-sum LDPC decoding algorithm for 5G new radio," in *Proc. International Symposium on Electrical and Electronics Engineering (ISEE)*, Ho Chi Minh, Vietnam, April 2021.

[18] J. Chen and M. P. C. Fossorier, "Density evolution for two improved BP-Based decoding algorithms of LDPC codes," *IEEE Communications Letters*, vol. 6, no. 5, pp. 208-210, 2002.

[19] R. Tanner, "A recursive approach to low complexity codes," *IEEE Transactions on Information Theory*, vol. 27, no. 5, pp. 533-547, 1981.

[20] M. P. C. Fossorier, "Quasicyclic low-density parity-check codes from circulant permutation matrices," *IEEE Transactions on Information Theory*, vol. 50, no. 8, pp. 1788-1793, 2004.

[21] A. Sassan, *5G NR: Architecture, Technology, Implementation, and Operation of 3GPP New Radio Standards*, Academic Press, 2019.

[22] R. Tom and S. Kudekar, "Design of low-density parity check codes for 5G new radio," *IEEE Communications Magazine*, vol. 56, no. 3, pp. 28-34, 2018.

[23] H. Cui, K. L. Trung, F. Ghaffari, D. Declercq, J. Lin, and Z. Wang, "An enhanced offset min-sum decoder for 5G LDPC codes," in *Proc. 25th Asia-Pacific Conference on Communications (APCC)*, Ho Chi Minh City, Vietnam, 2019, pp. 490-495.

[24] C. L. Wey, M. D. Shieh, and S. Y. Lin, "Algorithms of finding the first two minimum values and their hardware implementation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3430-3437, 2008.

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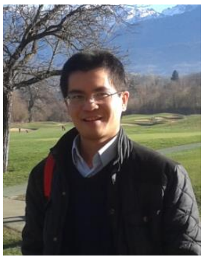

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