Self-Adaptive Rectenna with High Efficiency over a Wide Dynamic Range for RF Energy Harvesting Applications

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***Abstract*—This paper presents a novel simple adaptive and efficient rectenna with automatic power distribution to achieve high radio frequency-direct current (RF-DC) power conversion efficiency (PCE) over a wide range of RF input power. This design employs two rectifier paths operating at low and high-power levels, respectively. Automatic power distribution method exploits the power-dependent input impedance of the rectifier and routes the RF input power into the assigned path according to the input power level. A distinctive enhancement in the rectifier dynamic range is achieved when dividing the high path power equally into two or more parallel diode cells, which helps the high path to camouflage the diode breakdown voltage in case of high input power level. The proposed adaptive design applies two different rectifier topologies, one by using shunt diode topology and the other by using voltage doubler topology at 2.45 GHz. Simulated PCE of this work is kept above 50% over a range of 25.1 dBm from -5.7 to 19.4 dBm of RF input power using shunt diode topology and over a range of 30 dBm from -6.3 to 23.7 dBm of RF input power using voltage doubler topology.

***Index Terms*—RF energy harvesting, rectifier, automatic power distribution, power conversion efficiency

I. INTRODUCTION

Radio frequency harvesting (RFH) recycles the surrounding free energy and converting it into useful Direct Current (DC) voltage to power the low-power applications such as Wireless Sensor Network (WSN) and Internet of Things (IOT). Rectenna is the vital stage of RF energy harvester, it includes (antenna, impedance matching network, and rectifier) [1]. The overall performance of RF harvester is measured by many parameters such as RF-DC power conversion efficiency (PCE), sensitivity, operation distance, and output power. PCE of rectenna is defined as the ratio between rectenna DC output power measured on the load terminals (P_{out}) and the RF power captured by the antenna (P_{in}). Enhancing PCE is a challenging topic in the research field, each part of rectenna stage contributes in PCE enhancement. Improvement of antenna parameters includes polarization [2], gain [3], antenna impedance [4]. Matching impedance techniques presented to keep RF harvested power with minimum losses [5], [6], and different rectifier topologies applied to improve PCE [7].

PCE enhancement is achieved by improving the PCE maximum point value at a specific RF input power as presented in the previous literature, also it is introduced by keeping an acceptable value of PCE over a wide range of RF input power which is more vital for RF harvesting applications which does not depend on a dedicated RF source, as the surrounding RF power varies according to its location from the harvester and the time during the day.

Increasing PCE over a wide range of input power was presented in several studies. For example, self-tuning matching network proposed [8], increasing the diode breakdown voltage [9], using the resistance compression technique (RCT) [10], [11], applying the maximum power point tracking (MPPT) technique [12], and promising results were achieved using adaptive power distribution method [13].

The relation between PCE and RF input power is highly nonlinear, specifically as RF input power increases. PCE increases to reach its maximum value at the saturation point then decreases significantly [14] as illustrated in Fig. 1. Diode Rectifier saturation point depends on diode breakdown voltage. If the input voltage of the diode is controlled to be below the breakdown voltage over the power range of interest, the PCE over this range will be kept away from the saturation point.

As shown in Fig. 2, this work proposes two paths for RF input power depending on the power level. As the rectifier input impedance varies with input power, low path uses a matching impedance network optimized at low power level, and the high path uses a matching impedance network optimized at high power level. Low and high matching networks make the input impedances of low and high paths changes inversely with each other; this distributes the input power automatically between the two paths depending on the input power level. This design achieves an extensive enhancement in the rectifier dynamic range by dividing the high path power equally into two or more parallel diode cells by using Wilkinson power divider (WPD). Dividing the high power helps diodes to be away from the saturation point for extra input power range.

This paper is arranged in the next sequence. Section II presents a discussion of the proposed design parameters. The operating principle and simulation results of the

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proposed design are discussed in section III, and section IV presents the conclusion.

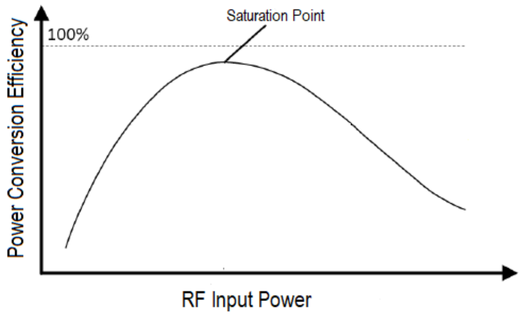


Fig. 1. Relation between rectifier power conversion efficiency and RF input power.

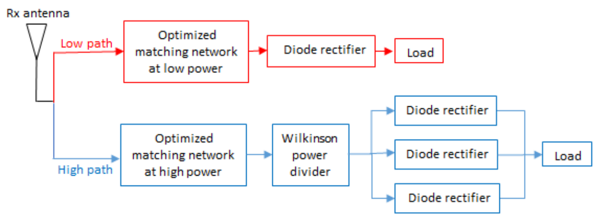


Fig. 2. Block diagram of proposed adaptive high PCE rectenna.

II. Design Parametres of the Proposed Design

Diode rectifier PCE saturation point depends on many parameters: as the breakdown voltage of selected diode, rectifier topology, and load resistance value. This section discusses the selection of diode and its effect on PCE, and rectifier topologies which are used in the proposed design.

A. Breakdown Voltage Effect

This study uses Schottky diode as a rectifying element due to its low turn-on voltage, the most popular diodes series used in rectenna are (HSMS285x and HSMS286x), each series has a different effect on PCE curve due to the difference in diode forward voltage V_F and diode breakdown voltage B_v as illustrated in Table I [15].

PCE is calculated using (1) and (2):

$$P_{out} = \frac{(V_{DC})^2}{R_{load}} \tag{1}$$

$$PCE = \left(\frac{P_{out}}{P_{in}}\right) \times 100\% \tag{2}$$

where V_{DC} is the output DC voltage, R_{load} is the applied load resistance.

The forward voltage V_F limits PCE in low input power levels, diode needs V_F as a minimum input voltage to turn

TABLE I: OPERATING PARAMETERS OF HSMS-285X AND HSMS-286X SCHOTTKY DIODES

Parameter	units	HSMS-285x	HSMS-286x
B_v	V	3.8	7
V_F at I_F=0.1 mA	mV	150	250
V_F at I_F=1 mA	mV	250	350

on the diode, so the lower values of V_F lead to better PCE in low input power levels.

The breakdown voltage B_v has a direct effect on the maximum DC output voltage and DC output power as illustrated in (3) and (4) [16]:

$$V_{DC\ \max} = \frac{B_v}{2} \tag{3}$$

$$P_{DC\ \max} = \frac{(B_v)^2}{4R_{Load}} \tag{4}$$

where V_{DCmax} is the maximum DC output voltage, P_{DCmax} is the maximum DC output power. Using Table I and (3), the estimated maximum DC output voltage for (HSMS-2850) is 1.9V and for (HSMS-2860) is 3.5V. To simulate the effect of the breakdown and forward voltages on the PCE curve, two rectifiers are simulated using Advanced Design System (ADS) software applying shunt diode rectifier topology optimized at 0 dBm input power. First rectifier by using an (HSMS-2850) diode and the second by using (HSMS-2860) diode with a load resistance of 1KΩ applied on each of them. Fig. 3 shows the simulation results of DC output voltage and PCE curve at 2.45GHz. In Fig. 3(a) at the breakdown voltage of each diode, the DC output voltage becomes steady. In Fig. 3(b), V_F effect makes a difference between PCE curves in the low RF input power levels, and B_v effect makes a shift in PCE saturation points that causes a difference between PCE curves in the higher RF input power levels.

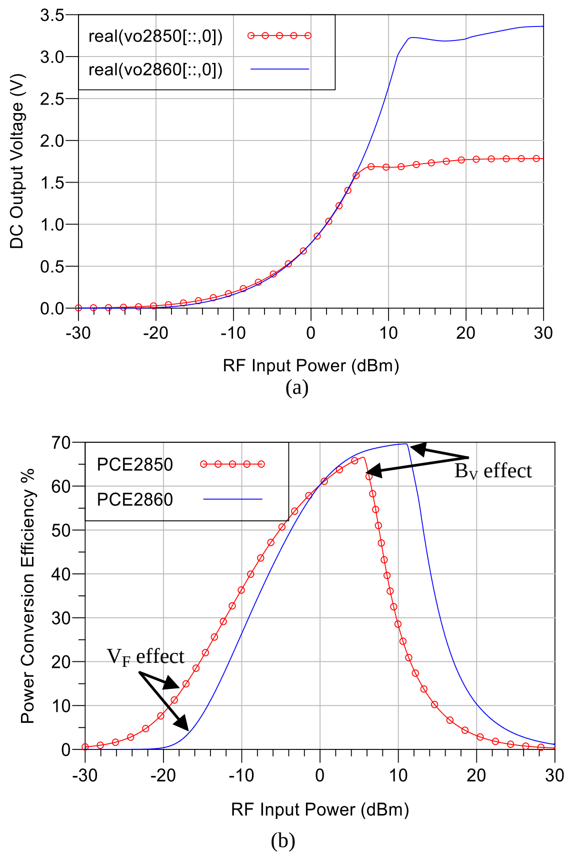


Fig. 3. (a) DC output voltage and (b) PCE of HSMS-2850 and HSMS-2860 rectifiers.

Table II summarizes the simulation results showed in Fig. 3. Simulated maximum output DC voltages are so close from the estimated values, the higher breakdown voltage of (HSMS-2860) makes a shift in the rectifier saturation point and achieves a wider power range (where PCE above 50%) than (HSMS-2850).

TABLE II: EFFECT OF BREAKDOWN VOLTAGE ON RECTIFIER BEHAVIOR.

Diode	HSMS-2850	HSMS-2860
Estimated V_{DCmax}	1.9 V	3.5 V
Simulated V_{DCmax}	1.78 V	3.35 V
Saturation point at	5.6 dBm	11 dBm
PCE range (above 50%)	12.7 dBm (from -5.2 to 7.5 dBm)	16.9 dBm from (-3.7 to 13.2 dBm)

The proposed design depends on dual path concept, one is dedicated for low input power levels and the other is dedicated for high input power levels. According to V_F effect, the (HSMS-2850) is selected for the low path as it has better values of PCE in the low power levels. According to B_v effect, the (HSMS-286x) is selected for the high path as it has better values of PCE in the higher power levels. So, switching between the two paths achieves an enhancement in the dynamic range of overall rectenna.

B. Rectifier Topology Effect on PCE

There are many rectifier topologies presented in the RF harvesting research field. The difference between them depends on the position and number of used diodes. The simplest topologies used are series or shunt mounted single diode [17], and they showed good performance in low power levels. Voltage multiplier or voltage doubler is also common in the literature to improve DC output voltage [18].

The proposed dual path adaptive rectenna introduces two designs. Both use shunt diode topology for the low-power path, but the high-power path uses shunt diode topology in one design and voltage doubler topology in the other design.

Fig. 4 shows the difference in DC output voltage and PCE between shunt diode rectifier topology using (HSMS-2850) diode and voltage doubler rectifier topology using (HSMS-2862) package.

In Fig. 4(a), voltage doubler topology introduces a high maximum DC output voltage in high input power levels. And Fig. 4(b) shows a remarkable shift between the saturation points and a wider dynamic range for the voltage doubler rectifier topology.

III. OPERATING PRINCIPLE AND SIMULATION RESULTS

The proposed design uses automatic power distribution method to route the RF input power to the low or high path according to input power level. The first part of this section discusses how the automatic power distribution method is applied on the proposed design, and the second part introduces the simulation results of the proposed design and shows the remarkable effect of dividing the high path into two or more parallel diode cells on the overall rectenna power conversion efficiency. This work proposes two designs applying two different rectifier topologies; one uses shunt model diode topology for both paths; and the other design uses shunt model diode topology in the low path and voltage doubler topology in the high path.

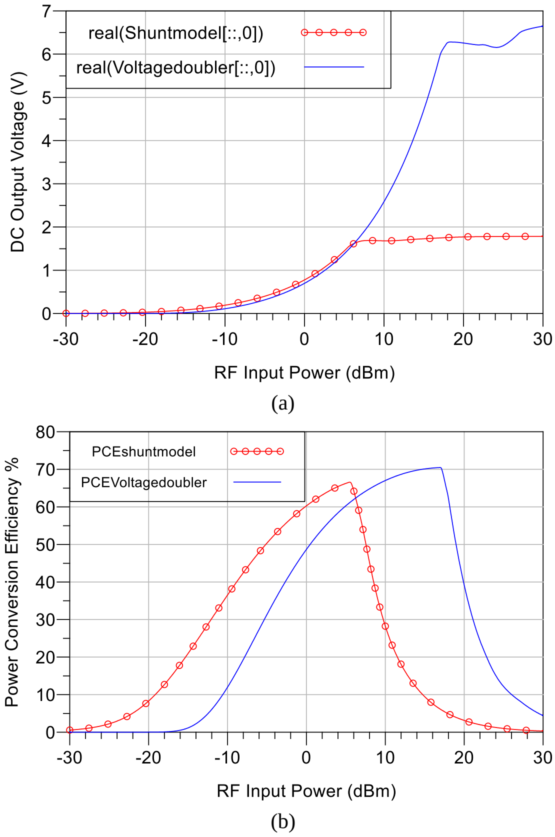


Fig. 4. (a) DC output voltage and (b) PCE of shunt diode rectifier topology and voltage doubler rectifier topology.

A. Operating Principle of the Proposed Rectenna

Fig. 5 shows a simplified schematic of the proposed design. Automatic power distribution method exploits the power-dependent input impedance of the rectifier.

Input impedance of low path is measured at low power level (-15 dBm), and a matching impedance network is designed to match it to the source impedance Z_S, while the input impedance of high path is measured at high power level (15 dBm) to design its matching impedance network to match the source impedance Z_S. The automatic power distribution takes a place when the input impedance of the two paths changes inversely with each other.

A stub matching network with the aid of an inductor or a capacitor are optimized for each path to achieve two goals. The first goal is to cancel the imaginary part of the path input impedance over the input power range of interest, and the second goal is to make the real part of low path input impedance R_{low} changes inversely with the real part of high path input impedance R_{High}. These two goals realize the automatic power distribution.

As illustrated in Fig. 5, the real part of low path input impedance R_{Low} increases with input power while the real part of high path input impedance R_{High} decreases with input power over the power range of interest. The main key of automatic power distribution is the inversely change of R_{Low} and R_{High} with the input power. This method introduces minimum losses when the input impedance of overall rectenna Rin is kept at value of 50 Ω over the targeted input power range using (5), the input power is distributed according to impedance ratio in (6):

$$R_{in} = R_{Low} // R_{High} = Z_s = 50\Omega \tag{5}$$

$$\frac{P_{Low}}{P_{High}} = \frac{R_{High}}{R_{Low}} \tag{6}$$

where P_{Low} and P_{High} are the input powers of low and high paths, respectively.

Applying (5) and (6), low path is activated only over low power ranges then with increasing of the input power, low path is deactivated and input power is switched to the high path over the higher power ranges. And the overall PCE of the proposed rectenna is calculated using (7):

$$PCE = \frac{\left(P_{DCLow} + P_{DCHigh}\right)}{P_{in}} \tag{7}$$

where P_{DCLow} and P_{DCHigh} is the DC output power of low and high paths, respectively.

This work aims to achieve an extensive enhancement in rectenna dynamic range by dividing the high path power into two or more rectifier cells. At high input power levels, the diode is about to reach its breakdown voltage and PCE saturation point, so dividing the high path power decreases the input voltage delivered to each divided cell and this makes the diode input voltage away apart from the breakdown voltage therefore achieves a wider dynamic range.

B. Simulation Result of the Proposed Design

This part shows the effect of dividing the high path power into two or more parallel diode cells on the overall rectenna power conversion efficiency, then the simulation results of the proposed design are introduced using two different topologies and finally compares the proposed design with the other works.

The simulation setup is created in the Agilent Advanced Design System (ADS) software because it is more suitable for microwave elements more than other simulation software like PSpice. Simulation is based on the use of RT/Duriod 6006 substrate from Rogers corporation [19] having a thickness of 0.635 mm, the relative dielectric constant is 6.15, and a metal thickness of 35 µm.

1) Effect of dividing the high path power on PCE

The high path is simulated separately, as Fig.6 shows the effect of dividing the high path input power, Wilkinson power divider (WPD) is selected among many simple power divider designs because it is a very low loss divider when the output ports are matched and the isolation resistors used introduces minimal loss, especially when microstrip transmission lines are used along with low-loss PCB substrate material [20] [21].

The simulation is achieved at first by using shunt diode model rectifier and then by using voltage doubler rectifier topology. The results show PCE in case of no power divider is applied (PCE_{ND}), applying two-way WPD (PCE_{D2}), and applying three-way WPD (PCE_{D3}).

Table III summarizes the simulation result showed in Fig. 6.

TABLE III: EFFECT OF DIVIDING HIGH PATH POWER ON PCE

Topology		No divider	Two-way WPD	Three-way WPD
Shunt diode model	PCE peak	65.4% at 11.1 dBm.	79.34% at 13.2 dBm.	79.22% at 16 dBm
	Power range for PCE >50%	10.5 dBm (from 2.6 dBm to 13.1 dBm)	13.9 dBm (from 2.2 dBm to 16.1 dBm)	16.9 dBm (from 2.7 dBm to 19.6 dBm)
Voltage doubler	PCE peak	79.4% at 13 dBm.	77.9% at 17.3 dBm.	77.7% at 20.3 dBm
	Power range for PCE >50%	16.1 dBm (from 0.4 dBm to 16.5 dBm)	17 dBm (from 3.4 dBm to 20.4 dBm)	18.2 dBm (from 5.6 dBm to 23.8 dBm)

The results in Table III highlight two main changes in PCE curve. First, an enhancement in PCE range is achieved according to PCE_{D2} and PCE_{D3} compared to $PCE_{ND.}$ Second change, PCE saturation point is shifted away in case of PCE_{2D} and PCE_{D3}. This shift helps to enhance the overall PCE of proposed rectenna as shown in Fig. 7, the saturation points of low and high path should be somewhat far away to reach the targeted wide dynamic range.

2) Simulation results using shunt diode rectifier topology

The simulation results of proposed design showed in Fig. 5 applying shunt diode rectifier topology for both paths are introduced in Fig. 8 by using single high path branch, Fig. 9 by using two-way WPD to divide the high path power into two rectifier branches, and Fig. 10 by using three-way WPD.

First, the simulation occurs using (Large Signal S-Parameter) LSSP simulator because it considers the nonlinearity of the diode. It measures the input impedance of the rectifier and designs the matching stub at the aimed power level. Next, optimization of the matching stub length occurs to get a good value of input reflection coefficient S11. Finally, a harmonic balance simulator (HB) is used to get the rectifier PCE.

In the optimization step, low path matching network is optimized at -15 dBm and high path matching network at

15 dBm. In case of dividing the high path, each rectifier cell is optimized at 7.5 dBm when using two-way WPD and optimized at 5 dBm when using 3-way WPD.

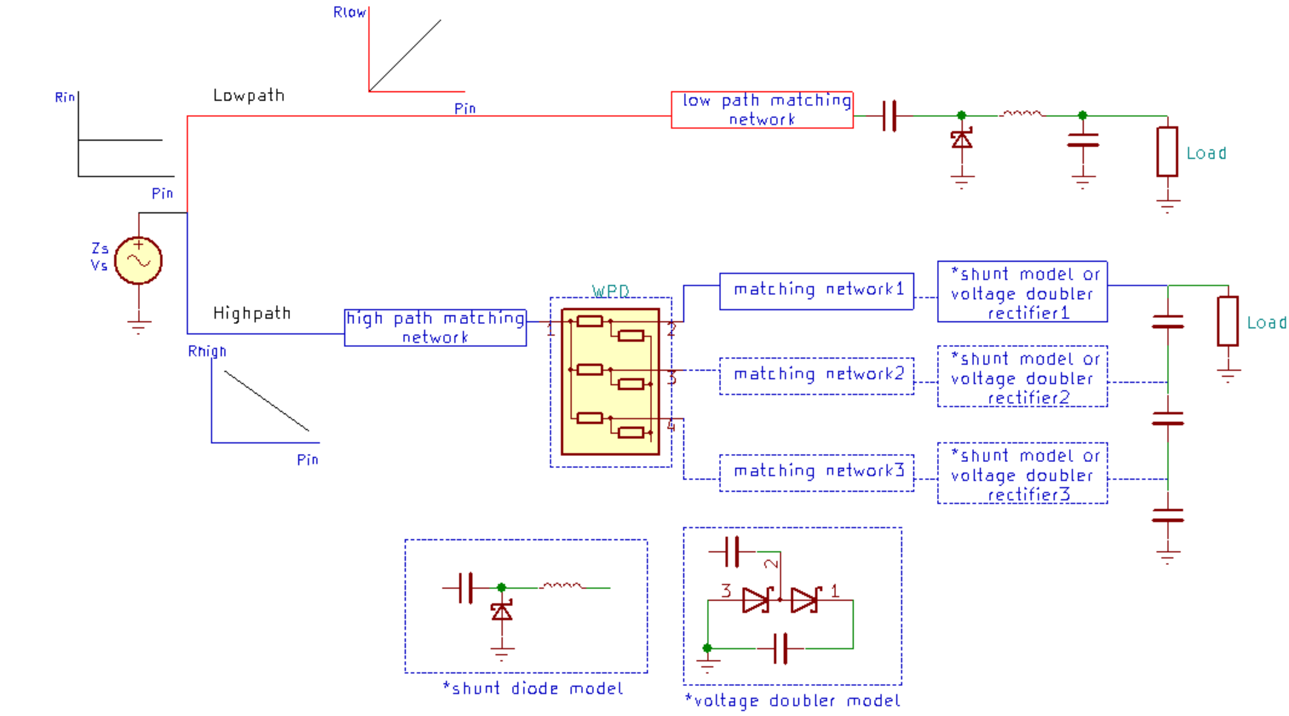
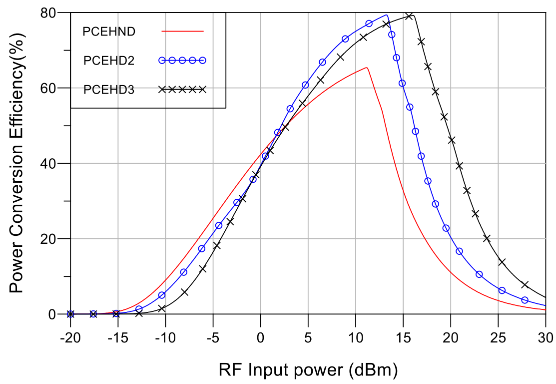
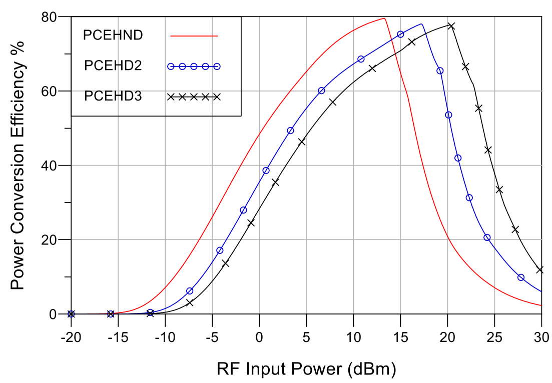


Fig. 5. The simplified schematic diagram of the proposed design.



(a)



(b)

Fig. 6. Effect of dividing the high path on PCE (a) applying shunt diode rectifier topology (b) applying voltage doubler rectifier topology.

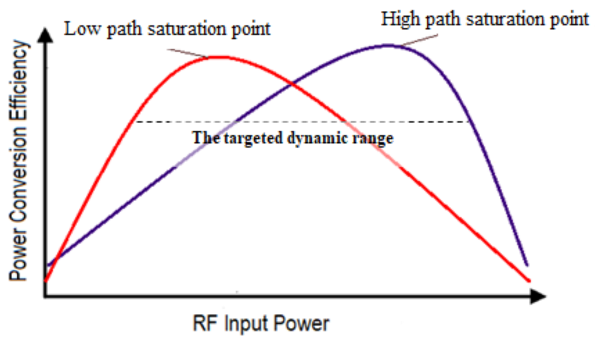


Fig. 7. Low and high path saturation points and the targeted dynamic range.

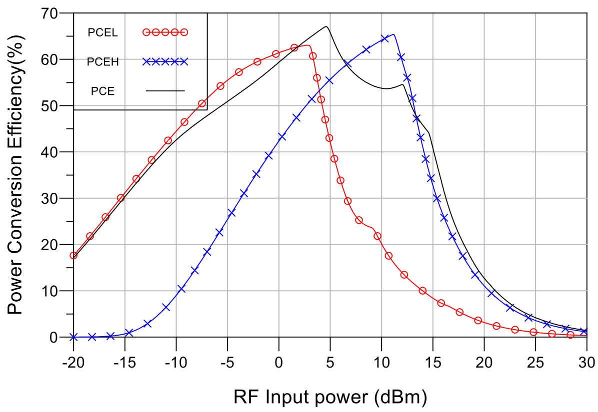


Fig. 8. PCE of the proposed design using shunt diode rectifier topology with applying single high path branch.

S11 of overall rectenna is kept below -10 dB for a wide range due to apply automatic power distribution conditions as shown in Fig. 11.

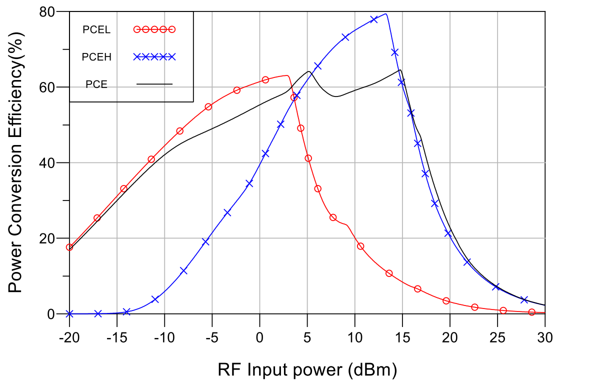


Fig. 9. PCE of the proposed design using shunt diode rectifier topology with applying two-way WPD.

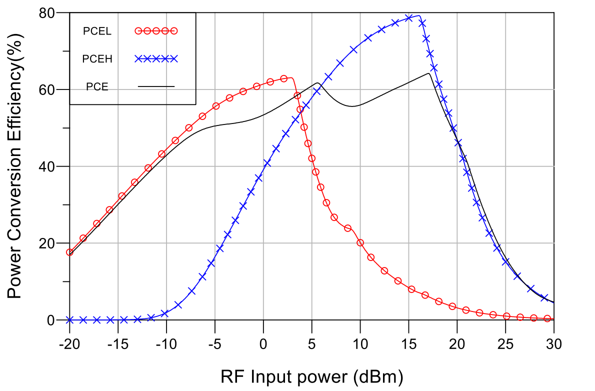


Fig. 10. PCE of the proposed design using shunt diode rectifier topology with applying three-way WPD.

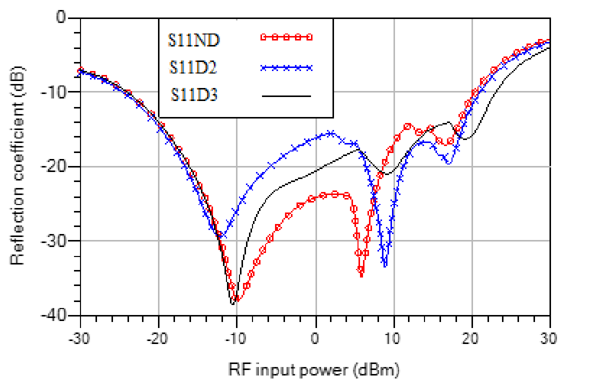


Fig. 11. Reflection coefficient S11 for the overall rectenna.

Each of Fig. 8, Fig. 9, and Fig. 10 introduces three PCE curves. PCEL indicates power conversion efficiency of low path, PCEH indicates power conversion efficiency for high path and PCE indicates the overall rectenna power conversion efficiency when the automatic power distribution routes the RF input power from low path to the High path. Fig. 11 shows S11 of overall rectenna, $S11_{ND}$ in case of no divider applied, $S11_{D2}$ applying two-way WPD, and $S11_{D3}$ applying three-way WPD, the results show more than 40 dBm power range for S11 < -10 dB.

3) Simulation results by using voltage doubler rectifier topology

This part introduces the simulation results of PCE when applying the voltage doubler rectifier topology in the high path rectifier cells and keeping the shunt diode rectifier topology in low path. Fig. 12, Fig. 13, and Fig. 14 show results in case of single high path branch, using two-way WPD, and using three-way WPD, respectively.

Fig. 15 shows S11 of overall rectenna, the results show more than 40 dBm power range for S11 < -10 dB.

A summary of the proposed design results from Fig. 8 to Fig .10 and from Fig. 12 to Fig. 14 are listed in Table IV. The results show an enhancement in the proposed rectenna dynamic range with keeping PCE above 50%, minimum power range for PCE > 50% is achieved through applying single high path using shunt diode rectifier for both paths, and the maximum power range for PCE > 50% is achieved by using three voltage doubler rectifiers in high path connected to shunt diode rectifier in the low path.

This paper proposes an efficient rectenna with wide dynamic range and achieves a remarkable enhancement in PCE value in the lower power levels as it has PCE of 30 % at -15 dBm which counts a good improvement as the next comparison illustrates.

Table V summarizes a comparison with previous works done to improve PCE over the range of RF input power. G. C. Martins and W. A. Serdijn applied MPPT to accommodate for the variation of input power by controlling the system, their design aimed to achieve wide dynamic range start at a very low input power, 11.2 dBm power range is achieved with keeping PCE above 40% but not extended for higher power levels [12]. A. S. Almansouri, M. H. Ouda and K. N. Salama used a variable biasing technique and kept PCE above 50% over 15.2 dBm of input power from (-29.788 dBm to -14.559 dBm), their enhancement did not extend to higher levels of input power [22]. X. Wang and A. Mortazawi achieved a wide dynamic range by applying automatic power distribution technique, 20.4 dBm power range achieved from (-1.4 dBm to 19.1 dBm) with keeping PCE above 50% using two diode rectifiers, their design not working below -5 dBm as PCE is zero at lower input power level than -5 dBm [13]. Z. Zeng, J. J. Estrada-López, M. A. Abouzied and E. Sánchez-Sinencio used multistage reconfigurable rectifier to switch the rectifier topology from series to parallel topology depending on the input power level, 14 dBm power range for PCE above 20% is achieved from (-16 dBm to -2 dBm) [23]. while this paper presents a promising simulation results for high PCE over a wide power range using automatic power distribution method, 18.5 dBm power range is achieved as a minimum achievable result for the proposed design with keeping PCE above 50% (from -5.6 dBm to 12.9 dBm) using two diode rectifiers, it keeps working at lower input power levels as it has PCE of 30% at -15 dBm , and the maximum achievable result for the proposed design is reached by using four diode rectifiers and achieves 30 dBm power range with keeping PCE above 50% (from -6.3 dBm to 23.7 dBm) and has PCE of 30 % at -15 dBm which make this design promising for RF energy harvesting application.

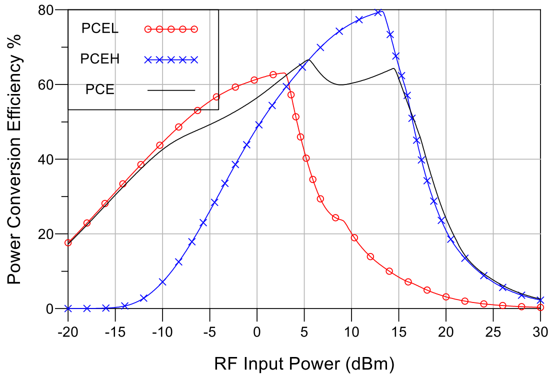


Fig. 12. PCE of the proposed design using voltage doubler rectifier topology with applying single high path branch.

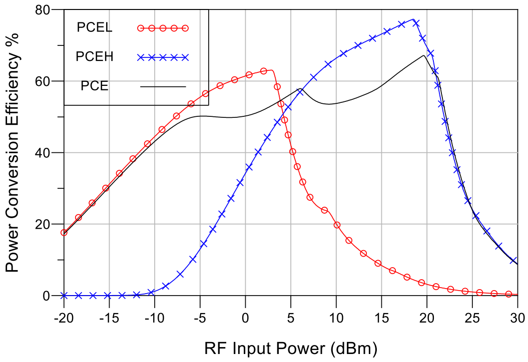


Fig. 13. PCE of the proposed design using voltage doubler rectifier topology with applying two-way WPD.

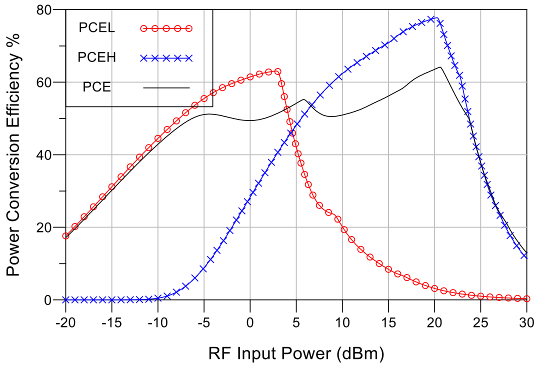


Fig. 14. PCE of the proposed design using voltage doubler rectifier topology with applying three-way WPD.

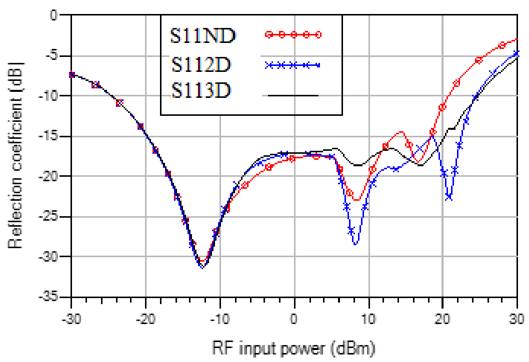


Fig. 15. Reflection coefficient S11 for the overall rectenna.

TABLE IV: SUMMERY OF THE PROPOSED DESIGN RESULTS

High path rectifier topology		Shunt diode	Voltage doubler	Overall No. of diode rectifiers
No divider	*PCE >50%	18.5 dBm (from-5.6 dBm to 12.9 dBm)	21.1 dBm (from -4.4 dBm to 16.7 dBm)	Two
	**PCE >30%	31.3 dBm (from-15 dBm to 16.3 dBm)	34 dBm (from-15 dBm to 19 dBm)	
Two-way WPD	*PCE >50%	20.4 dBm (from-4.1 dBm to 16.3 dBm)	27.7 dBm (from -5.6 dBm to 22.1 dBm)	Three
	**PCE >30%	33.9 dBm (from-15 dBm to 18.9 dBm)	39 dBm (from -15 dBm to 24 dBm)	
Three-way WPD	*PCE >50%	25.1 dBm (from -5.7 dBm to 19.4 dBm)	30 dBm (from -6.3 dBm to 23.7 dBm)	Four
	**PCE >30%	37.5 dBm (from-15 dBm to 22.5 dBm)	42.4 dBm (from-15 dBm to 27.4 dBm)	

*Power range with keeping PCE above 50%
** Power range with keeping PCE above 30%

TABLE V: COMPARISON WITH THE PREVIOUS WORK

Pub.	Methodology	Freq.	Peak PCE	PCE range	Result
[12]	MPPT	403.5 MHZ	49.1%	*11.2 dBm above 40%	simulated
[22]	Variable biasing technique	433 MHZ	*70%	*15.2 dBm above 50%	simulated
[13]	Automatic power control	900 MHZ	*65%	*20.4 dBm above 50%	simulated
[23]	Reconfigurable rectifier stage	820 MHz	39%	14 dBm Above 20% PCE	measured
This work	Automatic power control	2.45 GHz	67%	18.5 dBm above 50% PCE	simulated
This work	Automatic power control	2.45 GHz	62%	30 dBm above 50% PCE	simulated

*Estimated from the figure.

IV. CONCLUSION

This paper introduces a novel adaptive rectenna based on automatic power distribution technique for RF energy harvesting applications. It aims to keep high PCE over a wide range of RF input power. This design employs two rectifier paths operating at low and high-power levels respectively, and a distinctive enhancement in the rectifier dynamic range is achieved when dividing the high path power equally into two or more parallel diode cells. The proposed rectenna is simulated using two different rectifier topologies, 50% PCE is achieved over a range of RF input power 18.5 dBm as a minimum achievable result using two diode rectifiers and maximum achievable result is reached by using four diode rectifiers and achieves 30 dBm dynamic with keeping PCE above 50%.

CONFLICT OF INTEREST

The authors do hereby declare that there is no conflict of interest whatsoever concerning this paper.

AUTHOR CONTRIBUTIONS

All the authors contribute equally to the implementation of such work, both for bibliographic research, the simulation and for drafting of the paper. All authors had approved the final version.

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