

A Hardware Efficient Preamble Detection Algorithm for Powerline Communication

Tobias Stuckenberg and Holger Blume

¹Institute of Microelectronic Systems, 30167 Hannover, Germany
Email: stuckenberg@ims.uni-hannover.de; blume@ims.uni-hannover.de

Abstract—Orthogonal frequency-division multiplexing (OFDM) systems are widely used in today’s packet based communication systems including wireless and powerline communications. The latter is of increasing interest for the use in smart grid applications or internet of things (IoT). Some of the OFDM systems use a preamble preceding to the transmitted packet header and data to perform time and frequency synchronization. Common approaches for the detection of this preamble are using the cyclic repetition of repeated preambles or the cross-correlation of the transmitted and the reference preamble. While providing good performance in the low signal-to-noise-ratio (SNR) channels, the cross-correlation is a very costly operation when it is implemented in hardware. The field of application for the powerline system is an environment featuring a very low SNR channel. Therefore, cross-correlation based preamble detection is chosen. To reduce the hardware size, the effect of quantization on the cross-correlation has been evaluated and a new side-lobe correlation algorithm (SLC) is introduced. The results of the simulation show an improvement of up to 5 dB in SNR for various single and multipath channels. The FPGA implementation results for the SLC algorithm demonstrate that the required hardware effort can be significantly reduced by a factor of three, while providing the same minimum SNR.

Index Terms—Cross-correlation, HomePlug, FPGA, powerline, preamble, OFDM.

I. INTRODUCTION

Smart grid applications have gained a lot of attention over the last decade especially with regard to internet of things (IoT). The idea of connecting domestic appliances to your home network by only using the power supply connector has been proposed in [1], [2].

To realize these ideas powerline modems are required, which are both small and reliable. Various powerline standards have emerged since the early 1990s such as HomePlug, HomePNA, Panasonic AV and IEEE 1901 [3], where the latter is a standard emerging from the previous due to the need of unification over the various standards. This work will focus on the HomePlug standard that is widely used in Europe and America. There are four standards published by the HomePlug Alliance namely HomePlug 1.0 in 2001 [4], HomePlug AV in 2005 [3], HomePlug AV2 in 2012 [5] and HomePlug Green PHY

in 2012 [6]. The latter is designed with a reduced PHY layer to fit the IoT needs of small area and low power consumption. Herein, we will focus on HomePlug 1.0 and HomePlug GreenPHY as the two smallest designs in the HomePlug Alliance standards.

Both standards are based on orthogonal frequency-division multiplexing (OFDM) systems, which contain a preamble followed by frame control information and payload data. The preamble is needed to perform time domain synchronization and correction of the carrier frequency offset (CFO) of the OFDM symbols. The effect of the miss-aligned symbols has been studied extensively in [7]. A lot of work has been carried out in the field of OFDM-based communication to correct the CFO, so the focus of this paper is on how to find the preamble in a noisy and disturbed time domain signal. Since we have no influence on the structure of the preamble, we are limited in the choice of options for recognition. One idea is to use a cross-correlation to find the preamble. This approach is robust against noise and channel influence but requires a high amount of area in hardware design.

Another approach that is widely used is the synchronization scheme reported by Schmidl and Cox [8]. This scheme results in a huge amount of memory due to the given structure of the preamble in the HomePlug standards. The goal of this work is to find an implementation that is small in terms of area and robust against noise and channel disturbance.

This paper is organized as follows: Section II shows the related work. In Section III, the effect of noise and channel impulse response to the auto-correlation peak is evaluated. In Section IV, the proposed side-lobe correlation algorithm used for peak detection improvement is presented. The hardware structure and implementation results are shown in Section V. A conclusion is given in Section VI.

II. RELATED WORK

In 1995 Pollet, Bladel and Moeneclaey [9] have shown the sensitivity of OFDM systems to CFO. Since then various methods for synchronization and CFO estimation methods have been proposed and studied intensively. Recently Liu *et al.* [10] published an article, which classifies the synchronization techniques in preamble added and blind estimation algorithms. This paper focuses on the preamble added techniques because

Manuscript received July 17, 2017; revised January 10, 2018.
Corresponding author email: stuckenberg@ims.uni-hannover.de.
doi:10.12720/jcm.13.1.1-7

HomePlug systems all have preambles defined in the standard.

The preamble added techniques can again be separated into three different subcategories. First, there are the self-correlation algorithms initially proposed by Schmidl and Cox [8] in 1997. Many improvements to the idea of Schmidl and Cox have been made until today. There has been a publication by Minn, Zeng and Bhargava [11] who proposed an idea of how to remove the plateau of uncertainty presented in Schmidl and Cox. In 2003, Park, Cheon, Kang, and Hong [12] came up with the idea of symmetric correlation and introduced a peak estimator with very low side-lobe distortion. All these approaches can be implemented with a relatively low amount of hardware, but have a high mean squared error when compared to the cross-correlation based techniques. The second category uses the cross-correlation between the preamble and received signal. Kang, Kim, Ahn and Lee [13] defined an estimator, which multiplies a circular shifted version of the preamble with the original to create a correlator with high peak-to-side-lobe ratio. Yang, Zhang, Yu and Chen [14] and Abdzadeh-Ziabari and Shayesteh [15] improved the idea of Kang by using more cross-correlation terms and therefore, increased the number of calculations needed.

The last category is the combined self and cross-correlation approaches. Abdzadeh-Ziabari and Shayesteh [16] introduced an algorithm, which works independent of the preamble structure. Liu, Yu, Ji, Chen and Pan [17] improved their work by reducing the computational complexity by about 50%.

The algorithm introduced in this paper addresses the second class of cross-correlation based approaches. Since the structure of the preambles used in the HomePlug standards [3]-[5] is very different when compared to the ones used in IEEE802.11, which are used in most of the works mentioned above, there is a need for an approach independent of the preamble structure. For this idea, we first reevaluated the influence of noise and channel properties to the auto-correlation in the following section.

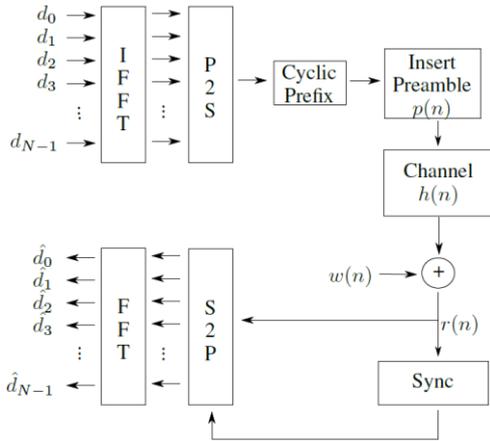


Fig. 1. The OFDM-based system model of transmission. The synchronization performed on the channel influence and additive white Gaussian noise (AWGN).

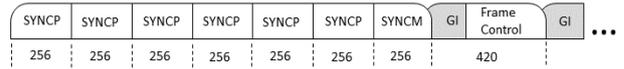


Fig. 2. The structure of the HomePlug 1.0 preamble and the subsequent frame control. The whole preamble consists of seven identical segments with 256 samples. The SYNCP are segments with a positive sign and the SYNCM are segments with a negative sign.

III. SYSTEM DESIGN AND ANALYSIS

The system for transmission used in this paper is shown in Fig. 1. We assume an OFDM-based system using a preamble for synchronization and additive white Gaussian noise (AWGN). The use of AWGN as an applicable source of noise for powerline channels, in the frequency range from 2 MHz to 25 MHz, is shown in [18], [19]. A cyclic prefix is added as the guard interval (GI) prior to every OFDM symbol but not to the preamble. The synchronization at the receiver triggers the serial-to-parallel (S2P) converter upon finding a preamble on the transmission channel indicating the first sample of each new symbol.

The structure of the HomePlug 1.0 preamble is shown in Fig. 2. The six SYNCP symbols are the 256 samples reference preamble given in the HomePlug 1.0 standard. The preamble is designed to have a sharp auto-correlation peak and covers the frequency range from 2 MHz to 25 MHz. The SYNCM symbol is identical to the SYNCP symbol but with a negative sign. The noisy and channel distorted SYNCP and SYNCM symbols are used as input data to the synchronization for the remainder of this paper.

$$r(n) = p(n) * h(n) + w(n) \quad (1)$$

The received preamble $r(n)$ at the synchronization can be expressed as shown in (1), where $p(n)$ is the reference preamble known at the transmitter and receiver, $*$ denotes the convolution of the channel impulse response (CIR) $h(n)$ with the transmitted preamble and $w(n)$ is AWGN. In this paper, we focus on the cross-correlation as an algorithm for timing estimation using only the preamble given above.

Equation (2) shows the discrete cross-correlation as a mathematical function.

$$C(\tau) = \sum_{n=0}^{N-1} p(n)r(n-\tau) \quad (2)$$

where N denotes the length of the preamble sequence, which is $N = 256$ in the case of the HomePlug 1.0 preamble. Our idea is to use the structure of the auto-correlation function to improve the ratio between the peak and side-lobes with a new side-lobe correlation (SLC) metric shown in Section IV. Therefore, we will evaluate the influence of noise and CIR on the shape of the auto-correlation peak in this section. We can rewrite the cross-correlation function in (2) as the auto-correlation and cross-correlation parts shown in (3).

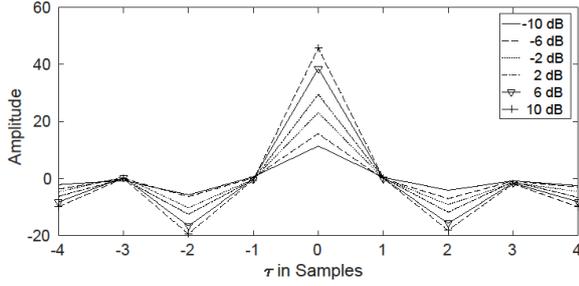


Fig. 3. The auto-correlation peak over the influence of the signal-to-noise ratio (SNR). The amplitude decreases with the decreasing SNR values.

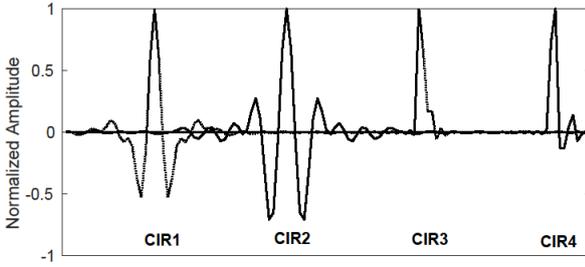


Fig. 4. The channel impulse responses used in this paper. CIR1 and CIR2 show the single transmitter-receiver pair channel with a length of 40 m for CIR1 and 100 m for CIR2. CIR3 is a 3-tap and CIR4 a 5-tap Rayleigh fading channel impulse response.

$$C(\tau) = R_{p_n p_n}(\tau) R_{p_n h_n}(\tau) + R_{p_n w_n}(\tau) \quad (3)$$

$R_{p_n p_n}(\tau)$ is the auto-correlation function of the transmitted preamble $p_n(t)$ and $R_{p_n h_n}(\tau)$ and $R_{p_n w_n}(\tau)$ are the cross-correlation with the channel and noise, respectively. If we assume a system without noise and channel distortion, the cross-correlation $C(\tau)$ will be equivalent to the auto-correlation $R_{p_n p_n}(\tau)$.

Initially, we neglected the influence of the CIR and focused on the shape of the cross-correlation influenced by noise. Fig. 3 shows a window of nine samples around the peak of the HomePlug 1.0 preambles cross-correlated with a noisy version of itself. It can be seen that the main peak and side lobe amplitudes are decreased with an increase in the SNR but the peak positions and therefore, the shape of the cross-correlation is not influenced.

Let us now consider the influence of the different CIRs on the cross-correlation of the preamble. In this paper, we will use four different CIRs modeling four typical situations on powerline channels. The first impulse response shown in Fig. 4 is a measured powerline channel with a length of 40 m using a single transmitter-receiver pair. The second CIR is a measured 100 m powerline channel also with a single transmitter-receiver pair. CIR3 and CIR4 are simulated multipath Rayleigh fading channels with three reflections for CIR3 and five reflections for CIR4. The suitability of Rayleigh fading channels for powerlines has been shown in [19]. All impulse responses have been normalized for comparison of the side-lobe shapes.

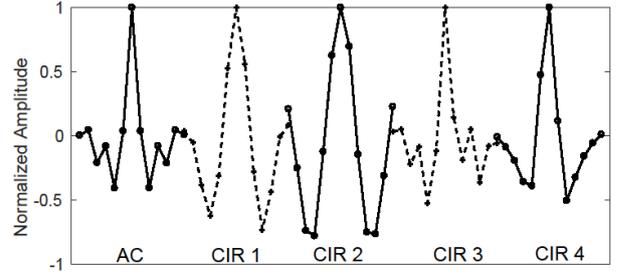


Fig. 5. The cross-correlation peaks influenced by the CIRs. Each plot is shifted to increase the visibility and shows 13 samples centered at the peak position.

The shape of the cross-correlations calculated at the receiver is shown in Fig. 5, where CIR1-CIR4 refers to the channel impulse responses from Fig. 4. The AC peak at the most left position is the auto-correlation of the preamble, which is given as a reference for comparison. The cross-correlations under the influence of CIR1 and CIR2 stretch the correlation peak over several samples resulting in a wider peak. The side-lobe symmetry, which can be seen in the auto-correlation, is not influenced. For CIR3 and CIR4, the width of the peak is not spread symmetrically like in CIR1 and CIR2. Furthermore, the original auto-correlation is distorted only to the right side of the main peak by tilting the side-lobes depending on the number of reflections. Still there is a symmetry, which can be used in our new approach that correlates the side lobes.

IV. PROPOSED ALGORITHM

In this section, we propose a new algorithm to improve the peak pronunciation for peak detection using the symmetry shown in Section III. Our new approach was compared to the method of Kang, Kim, Ahn and Lee. [9] and the standard cross-correlation shown in (2). The results show a significant performance gain over the cross-correlation approach and a small gain when compared to Kang's algorithm.

Our new metric called SLC is an incremental step on cross-correlation. The correlation of the side-lobes will be added up with the results from cross-correlation in a correlation window. This function can be described mathematically as follows:

$$slc_{opt} = \frac{1}{2W} \sum_{i=1}^W C(\tau_{peak} - i) C(\tau_{peak} + i), \quad (4)$$

where slc_{opt} is the SLC metric, $C(\tau_{peak})$ is the position of the possible peak and $2W + 1$ is the size of the window with W samples for each the left-hand and right-hand correlation parts around the peak. Tests, which vary the length of $W \in [1; 20]$, show that $W = 4$ is optimal to capture the SLC and does not introduce significant overhead in additional computation complexity. The final threshold metric used in this paper is

$$t_{SLC} = C(\tau_{peak}) + \alpha slc_{opt}, \quad (5)$$

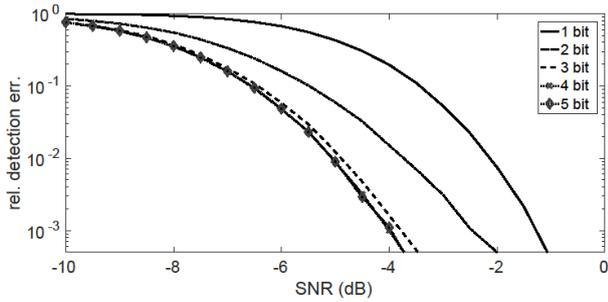


Fig. 7. The cross-correlation under the influence of the input quantization and SNR. More than 3 bit does not yield a significant improvement.

where α is a weighting factor greater than one, regulating the influence of the SLC on the peak metric. This factor has to be determined empirically for each preamble. For the HomePlug 1.0 preamble, $\alpha = 4$ was found to be the optimal weighting factor upon comparing the results of the peak detection at very low and very high SNR. The bigger α , the more false positive detections will be found at a high SNR.

To verify the robustness of our method we compared our approach against the existing approach of Kang, Kim, Ahn, and Lee [9], which is independent of the preamble structure. A shift value in Kang’s algorithm of $d = 2$ was found to be optimal for the given HomePlug 1.0 preamble. The algorithm used to determine d can be found in [13]. The method of Schmidl and Cox [8] or Ren, Chang, Zhang and Zhang [20] cannot be compared to our approach due to the absence of a GI and preamble structure, as shown in Fig. 2. Even though the approaches of Abdzadeh and Shayesteh [16], and Liu, Yu, Ji, Chen and Pan [17] yield better performance in terms of robustness they were not chosen for comparison since their computational complexity is far greater than Kang’s approach and therefore, not applicable for our application. An extensive study comparing the performance of all these approaches can be found in [10].

The results of the simulation are shown in Fig. 6 and consist of 10,000 runs at each value of SNR from -15 dB to 15 dB with an increment of 0.5 dB. The four different channels plotted in Fig. 5 were used for comparison. The ordinate shows the relative detection error on a logarithmic scale assuming either a missed preamble or detection when no preamble is present. The results are obtained by applying a threshold to the metric with an identical limit for each channel.

For CIR1, the SLC metric outperforms Kang’s metric and cross-correlation. Both Kang’s metric and the SLC can benefit from the symmetry of the CIR and yield about 5 dB and 7 dB better performance. For CIR2, the results are shifted by 3 dB for Kang and 5 dB for the SLC algorithm. Kang’s metric and the SLC metric are close to identical and outperform the cross-correlation by 10 dB. For the multipath channels, Kang’s metric performs worse than the SLC algorithm and cross-correlation approach. It can be seen that in both CIR3 and CIR4 the

SLC metric is about 3 dB better in detection performance when compared to the cross-correlation and more than 5 dB when compared to Kang’s metric.

The results of the simulation show that the performance gain greatly depends on the CIR but for all the cases shown the SLC algorithm performs better than Kang’s metric or the standard cross-correlation and is therefore an improvement in synchronization. In the following section, we show the implementation of these algorithms and discuss the trade-off between the hardware resources and detection ratio.

V. FPGA IMPLEMENTATION

For an implementation in hardware architecture, the number of bits required in order to achieve a sufficient algorithmic precision is of importance. The effect of quantization on the cross-correlation is shown in Fig. 7, where the influence of a CIR is neglected. It can be seen that more than $N_q = 3$ bit quantized input signals does not yield a significant benefit in the detection rate. Therefore, the implementations will be evaluated using 1 bit, 2 bit and 3 bit quantization. Since the SLC algorithm is an extension to the cross-correlation, we first show the hardware resources for the baseline correlation algorithm and then show the additional SLC correlation stage.

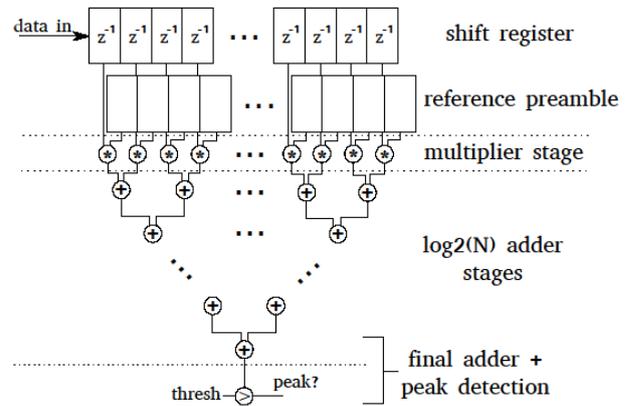


Fig. 8. The structure of the cross-correlation implemented in the hardware. The size of the shift register, the number of multipliers and adders depends on the length of the preamble. The peak detection was performed by thresholding the computed value.

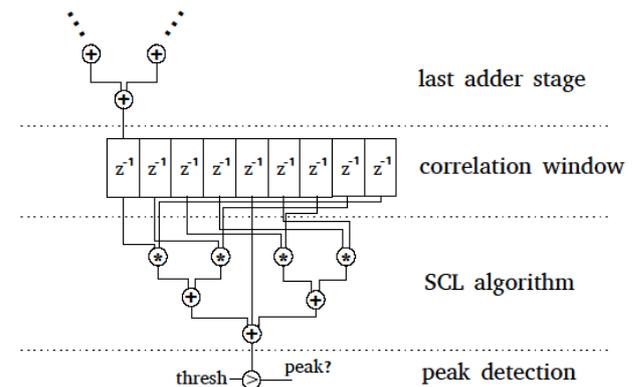


Fig. 9. The additional hardware stage for the SLC algorithm comprised of a 9-tap shift register, four multipliers and three adders.

Fig. 8 shows the structure of the cross-correlation implementation. The received samples are stored in a shift register and the reference preamble stored in constant registers. The word length of the registers and preamble depends on the chosen quantization. The following multiplier stage is used in combination with the reference preamble to create constant multipliers, which in case of 1 bit quantization are basic XOR-operations. The adder stages start at a word length of $2N_q$ bit and increase by 1 bit per stage resulting in $2N_q + \log(N)$ bit at the thresholding stage. N denotes the length of the preamble. The SLC stage shown in Fig. 9 is inserted after the last adder and prior to the thresholding in Fig. 8. Nine additional registers are needed to save the correlation results and four multipliers and four adders are inserted for SLC. The peak position found is four samples delayed because SLC has to be carried out for the right-hand side-lobe, which follows after the peak. Therefore, the incoming data stream is also delayed by four samples.

For comparison, the algorithm reported by Kang was also implemented. Less than 5 bit of quantization lead to the very poor performance of this algorithm. The structure of the algorithm is described in [13] and has been implemented using the shift register approach. The implementations were synthesized for a Xilinx Kintex-7 XC7K410TFFG900 FPGA with 410k look-up tables (LUT), which is part of the National Instruments PXIe-7975R module. The PXI system was used as a prototype platform for the powerline communication system and therefore, the synchronization algorithm runs on that platform as a part of the communication system. Synthesis is done using Vivado 2016.3 with area optimization option and without the use of the DSP-slices. The latter is carried out due to area comparison issues since the additional SLC stage makes use of the DSP-slices for side-lobe correlation but the cross-correlation part does not. The LUTs in this FPGA consist of six inputs (LUT-6). The synthesis results for 1 bit, 2 bit, 3 bit SLC and cross-correlation (CC) can be found in Table I. Kang's algorithm is only given using 5 bit input quantization since fewer bits yield a significant loss in the detection performance. It can be seen that the number of LUTs scales linearly with the number of bits used for the SLC and CC algorithm. Kang's algorithm has an implementation overhead of an additional shift register other than the SLC and CC algorithm, and is therefore nearly twice as large when comparing the 3 bit SLC implementation. Overall, the smallest design is the cross-correlation algorithm.

The frequency decreases because the critical path scales linear with the number of bits as well, as shown in Table I. The HomePlug 1.0.1 standard defines a frequency range of [0 MHz; 25 MHz], which has to be captured by an analog front-end (AFE) using at least 50 MHz as the sampling frequency. All the algorithms and

configurations are fast enough to keep up the targeted operational frequency.

Fig. 10 shows the combined results of algorithmic performance and hardware implementation. The SNR values were extracted from Fig. 6 for a maximum detection error rate of 10^{-3} , which can be seen in Table I. The optimum implementation is the bottom left corner, where the SNR has its maximum negative value and a minimal area is needed for the implementation. Fig. 10 is split into four sections showing the four CIRs for this paper and the data points are grouped by the amount of bits used as input quantization. It can be seen that for CIR1 and CIR2 the SLC algorithm outperforms Kang's algorithm in size and robustness against the SNR. It also outperforms the CC algorithm in robustness but not in size, which is obviously in regard to the additional space used for the SLC. For CIR3 and CIR4, the 1 bit SLC algorithm and the 1 bit CC algorithm are near to identical in terms of the SNR. In case of the 2 bit implementations, the SLC outperforms the CC algorithm for CIR4 but not for CIR3.

Overall, it can be seen that our new proposed algorithm outperforms Kang's algorithm in terms of area and robustness against the SNR. It works particularly well with the measured CIR1 and CIR2, and still slightly increases its robustness against the CC algorithm. One exception is the 3 bit version, which is about 3 dB in the SNR better than any of the other tested algorithms.

VI. CONCLUSIONS

In this paper, a new method to improve preamble detection in noisy powerline based environments has been proposed. The algorithm has been tested under various CIRs and SNR conditions, and the results show that the SLC algorithm works particularly well with a single transmitter-receiver pair. The SLC algorithm, Kang's algorithm and quantized cross-correlation have been implemented in a Xilinx Kintex-7 FPGA. The results show that the additional area for SLC is about 30%, but the maximum frequency increases by about 10 MHz.

TABLE I: SYNTHESIS RESULTS FOR A KINTEX-7 FPGA FOR NON-PIPELINED IMPLEMENTATIONS.

Name	FPGA Resource	
	#LUT	Max Frequency
1 bit CC	308	148 MHz
2 bit CC	624	125 MHz
3 bit CC	1357	106 MHz
1 bit SLC	431	158 MHz
2 bit SLC	846	136 MHz
3 bit SLC	1659	118 MHz
5 bit Kang	3433	76 MHz

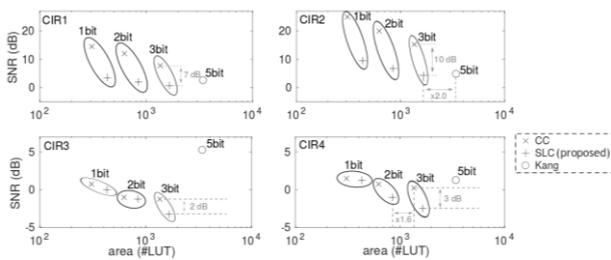


Fig. 10. The relationship between the SNR and required area in the number of LUTs. Both axes are given as a logarithmic scale. The SLC algorithm performs better or equal to the other algorithms using fewer input bits.

The frequency is high enough to keep up with the typical sampling rates observed for AFEs in powerline communication. The results show that for single path transmission systems the SLC algorithm with 1 bit of quantization yields better results than 3 bit quantized cross-correlation. Effectively, we can implement an equivalently performing system with about 30% of the area and 2 dB more robustness against the SNR when compared to the quantized cross-correlation. Kang’s algorithm has been shown to work well for single-user channels as well but has two times the area when compared to the SLC algorithm and is therefore not applicable for small IoT applications.

For multipath transmission systems, as in CIR4, the peak detection system of the new 2 bit-SLC algorithm yields a 2 dB better performance in the SNR than the 3 bit quantized cross-correlation and only needs half of the area.

ACKNOWLEDGMENTS

This work was supported by the German Research Foundation (DFG) under Grant No. INST 187/650-1 FUGG.

REFERENCES

[1] A. R. Al-Ali and R. Aburukba, “Role of internet of things in the smart grid technology,” *Journal of Computer and Communications*, vol. 3, no. 5, pp. 229-233.

[2] X. Li, R. Lu, X. Liang, X. Shen, J. Chen, and X. Lin, “Smart community: an internet of things application,” *IEEE Communications Magazine*, vol. 49, pp. 68-75, 2011.

[3] H. A. Latchman, S. Katar, L. Yonge, and S. Gavette, *Home Plug AV and IEEE 1901: A Handbook for PLC Designers and Users*, 1st ed., New Jersey, Wiley-IEEE Press, 2013, ch. 4, pp. 37-40.

[4] Home Plug 1.0 Specification, Home Plug Alliance Standard, Version 1.0.1, 2001.

[5] Home Plug AV2 Technology, Home Plug Alliance Standard, 2010.

[6] Home Plug Green PHY, Home Plug Alliance Standard, Version 1.1.1, 2013.

[7] Z. Cvetkovic, V. Tarokh, and S. Yoon, “On frequency offset estimation for OFDM,” *IEEE Transactions on Wireless Communications*, vol. 12, no. 3, pp. 1062-1072, 2013.

[8] T. M. Schmidl and D. C. Cox, “Robust frequency and timing synchronization for OFDM,” *IEEE Transactions on Communications*, vol. 45, no. 12, pp. 1613-1621, 1997.

[9] T. Pollet, M. V. Bladel, and M. Moeneclaey, “BER sensitivity of OFDM systems to carrier frequency offset and wiener phase noise,” *IEEE Transactions on Communications*, vol. 43, no. 2, pp. 191-193, 1995.

[10] Y. Liu, F. Ji, H. Yu, D. Wan, F. Chen, and L. Yang, “Robust preamble based timing synchronization for OFDM systems,” *Journal of Computer Networks and Communications*, vol. 1, pp. 1-7, 2017.

[11] H. Minn, M. Zeng, and V. K. Bhargava, “On timing offset estimation for OFDM systems,” *IEEE Communications Letters*, vol. 4, no. 7, pp. 242-244, 2000.

[12] B. Park, H. Cheon, C. Kang, and D. Hong, “A novel timing estimation method for OFDM systems,” *IEEE Communications Letters*, vol. 7, no. 5, pp. 239-241, 2003.

[13] Y. Kang, S. Kim, D. Ahn, and H. Lee, “Timing estimation for OFDM systems by using a correlation sequence of preamble,” *IEEE Transactions on Consumer Electronics*, vol. 54, no. 4, pp. 1600-1608, 2008.

[14] F. Yang, X. Zhang, W. Yu, and G. Chen, “Coarse symbol timing for OFDM systems by ranking preamble cross-correlations,” in *Proc. 47th Annual Conference on Information Sciences and Systems*, vol. 47, pp. 1-6, 2013.

[15] S. H. Abdzadeh-Ziabari, M. G. Shayesteh, and M. Manaffar, “An improved timing estimation method for OFDM systems,” *IEEE Transactions on Consumer Electronics*, vol. 56, no. 4, pp. 2098-2105, 2010.

[16] S. H. Abdzadeh-Ziabari and M. G. Shayesteh, “Robust timing and frequency synchronization for OFDM systems,” *IEEE Transactions on Vehicular Technology*, vol. 60, no. 8, pp. 3646-3656, 2011.

[17] Y. Liu, H. Yu, F. Ji, F. Chen, and W. Pan, “Robust timing estimation method for OFDM systems with reduced complexity,” *IEEE Communications Letters*, vol. 18, no. 11, pp. 1959-1962, 2014.

[18] O. G. Hooijen, “A channel model for the residential power circuit used as a digital communications medium,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 40, no. 4, pp. 331-336, 2002.

[19] M. Zimmermann and K. Dostert, “A multipath model for the powerline channel,” *IEEE Transactions on Communications*, vol. 50, no. 4, pp. 553-559, 2002.

[20] G. Ren, Y. Chang, H. Zhang, and H. Zhang, “Synchronization method based on a new constant envelop preamble for OFDM systems,” *IEEE Transactions on Broadcasting*, vol. 51, no. 1, pp. 139-143, 2005.



Tobias Stuckenberg received his Bachelor of Science in 2014 and Master of Science in 2016 both in Technical Informatics. Since 2016, he has worked at the Leibniz Universität Hannover in the Institute of Microelectronic Systems as a research engineer. His present research includes powerline based communication and its hardware architectures for harsh environments.



Holger Blume received his diploma in electrical engineering in 1992 at the University of Dortmund, Germany. In 1997, he achieved his Ph.D. with distinction from the University of Dortmund, Germany. Until 2008, he worked as a senior engineer and as an academic senior counselor at the chair of

electrical engineering and computer systems (EECS) of RWTH

Aachen University. In 2008, he achieved his postdoctoral lecture qualification. Holger has been a Professor for 'architectures and systems' at the Leibniz Universität Hanover, Germany, since July 2008 and manages the Institute for Microelectronic Systems. His present research includes algorithms and heterogeneous architectures for digital signal processing, design space exploration for such architectures as well as research on their corresponding modeling techniques.