# 3D Network-on-Chip Based Median Filter Implementation

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***Abstract***—This paper presents an efficient three dimension Networks-on-Chip (NoC) mesh topology which developed for digital image processing. The NoCs are emerging as a good solution for the communication of SoCs. With this advantage there is a significant growth of the number of cores or processing elements in a same chip. Communication between tens or hundreds of cores has become a main issue. We introduce developed 3D mesh topology for resolving this issue that is suitable for digital image processing. A 3D-Mesh is a generic, scalable and configurable topology which uses XYZ Dimension Ordered Routing (DOR) algorithm. We also implement a median filter to restore corrupted digital images. Our method for implementing the median filter is better and preferable compared to the implementation on a 2D mesh architecture. Experimental results show a significant improvement in execution clock cycle count for 3D mesh architecture which gets better while increasing the network size.

***Index Terms***—3D-Mesh; network-on-chip; core; topology; median filter

## I. Introduction

A system on a chip (SoC) is a microchip with all necessary components, integrated into a single chip. It may contain different parts, such as memory blocks, I/Os and other peripherals. SoC is a typical application in the area of embedded systems. Nowadays number of SoCs on a single chip increases rapidly and for this issue the communication overhead is an important problem.

Accordingly, Network on a Chip (NoC) has been emerged as a good candidate and platform for the on-chip communication systems [1]-[3]. 2 dimension NoCs has limited on chip communication performance [4]-[6]. Hopefully, 3D design topologies, such as 3D mesh NoCs, have been proved to be able to decrease communication overhead and improve NoC performance [4]-[9].

Due to the high processing overhead to recover a corrupted image, the use of fast processing platforms is required. In this regard, there are many ways and methods to retrieve a corrupted image. One of the best functions and techniques to restore the corrupted image is median filter. Digital processing of images performs image processing on digital images by various algorithms. Wide range of algorithms can be applied to the image data and avoid problems such as the build-up of image noise during processing.

Digital image processing filters have a significant role in image restoration. Therefore, filters are used to reconstruct the corrupted and noisy image. In this research work we implement a novel 3D mesh NoC based median filter which simply reconstructs impulse Salt & Pepper noise, while keeping other noise free pixels. Next section caries out a literature review on related works on 3D mesh NoC architectures and implementations. Section 3 provides a background for median filters. Section 4 and 5 introduce the implementation of our 3D NoC median filter in Heracles. Section 6 presents the simulation results and shows a performance comparison between 3D and 2D NoC topologies. Finally, we conclude our paper in section 7.

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## II. Related Works

NoCs employ suitable communication architectures in multi-processor SoC which provides parallelism, high performance and low power design [10], [11]. Several publications and papers have highlighted the NoC designs and its topologies, such as [12]. Tightly-coupled multi-layer topologies for 3D NoCs has proposed in [10] which called Xbar-connected Network-on-Tiers (XNoTs). Furthermore, [6] focus on a 3D mesh topology optimization for area and latency minimization. In [13] authors have proposed a reliable NoC based on generalized De Bruijn graph and a reliable routing algorithm to bypass the link faults. Reference [4] introduced and highlighted four 3D NoC architectures: 3D mesh, 3D BFT, ciliated 3D mesh and stacked Mesh as shown in Fig. 1.

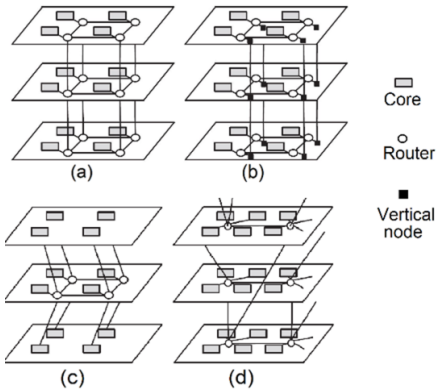


Fig. 1. 3D mesh and tree based network on chip, (a) 3D mesh, (b) stacked mesh, (c) ciliated 3D mesh and (d) 3D BFT [4].

A FPGA implementation of 2D Mesh and other topologies has been explained in [14]. They compare several topologies, different application and routing algorithms in every topologies and it gives FPGA resource utilization per mesh sizes. Reference [15] focuses on a novel 3D NoC architecture which is based

on De Bruijn graph. On the other hand, [16] proposed a fast and efficient median filter for removing Salt & Pepper noise in images. However, only a few papers focus on the simulation and implementation of median filters on NoCs and they do not implement 3D mesh NoC based median filter.

## III. Median Filter

In digital image processing field, noises seriously has a considerable effect on efficiency of image processing programs and applications [16]. Noise impact on digital images is a typical problem in most of these applications. [17]. Thus, median filter is a strong method to remove the impulsive noise from a specific image. This is a totally intensive operation. Also, it has a much higher computational cost [17]. Fortunately, 3D mesh NoC is a flexible and suitable platform for implementing median filter and will be solved most of the above issues to a satisfactory level.

In our median filtering procedure, for achieving the best result the minimum number of pixels in mask window must not be less than eight pixels and the other hand the large number of pixels in mask window collects general information from the image and reduces the accuracy of restoration [18]. So, we used a 3×3 pixels fixed mask window. Methods define that a square mask is moved around the image and at each stage, sampled pixels are stored in an array. At the end of each stage, median of these samples is stored in the center of the mask. Fig. 2 shows the median filter mechanism. Median of 9 pixels is located on the central coordinate of window of corrupted image.

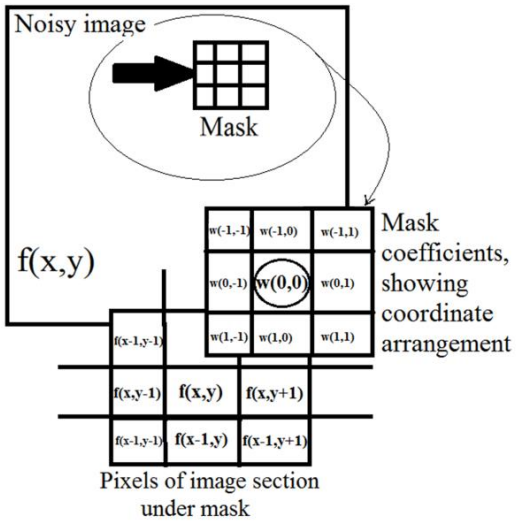


Fig. 2. Corrupted image and mask coefficients

## IV. NoC

Interconnections of on chip networks are rapidly becoming main topic in multi-core and multi-processor systems. Therefore, communication between many-core systems has become an important issue in high performance processors (HPP) [19], [20].

NoC was first proposed in [1] and it consists of cores, links or channels and switches. The most basic part of a switch is the router. So, in this paper, we do not need the details of a NoC switch and we modeled a switch with just its router part. In this paper we processed information is exchanged across routers, from source to destination core. NoC architecture is defined by its topology, which means the physical organization of switches or cores in network [14]. Also, another important parameter in a NoC is routing algorithm which determines the path to reach the destination. If this path is shorter, network latency and power dissipation will be less. Due to the network diameter, 3D mesh topology achieves low latency and power consumption. Fig. 3 shows a 4×2 2D mesh NoC high level model that contains cores, bidirectional channels and routers. In this model we don't show channel (links) or switches details.

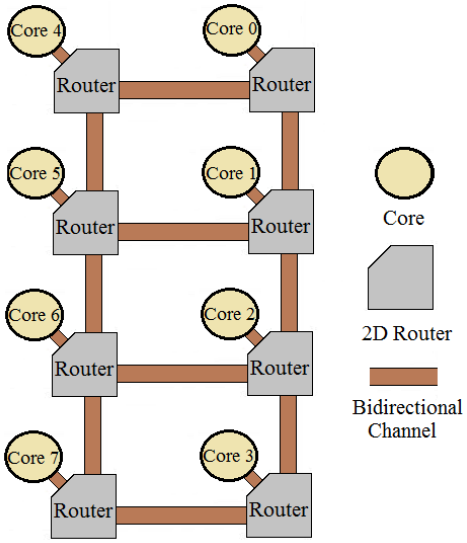


Fig. 3. A 4×2 2D mesh NoC model with routers, bidirectional channels and cores.

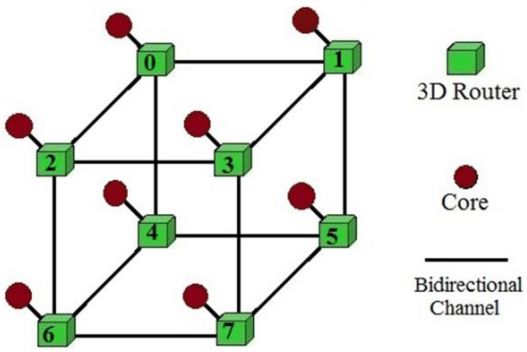


Fig. 4. A 2×2×2 3D mesh NOC model with 3D routers, bidirectional channels and cores.

Scaling on the chip network over two dimensions to establishing several cores is not efficient. Thus, there is a fundamental bottleneck and limitation on building long path and interconnection between cores [21]. In this kind of circumstances, 3D integration technologies have been emerged [11]. In Fig. 4 we show a 2×2×2 3D mesh based

NoC high level model. This architecture uses XYZ Dimension Ordered Routing (DOR) algorithm [22].

3D NoCs provide performance improvement, energy efficiency, size minimization, cost reduction and reconfigurable modular design [23]. For a large number of reasons, such as the use of through-silicon-via (TSV) technology [5] and the accumulation of silicon layers on top of each other and the creation of short communications between them, the use of 3D architectures reduces the length of communications and delays [24]. In addition, it reduces hop count from a given core to another. For example, in Fig. 4 from core 0 to core 7 we have 3 hops, but in 2D mesh shown in Fig. 3, we have 4 hops. Overall, from core 0 to other cores, we have 12 hops for 3D and 16 hops for 2D mesh which prove the effectiveness of 3D mesh NoC in our application. In this paper we developed a fully synthesizable 3D mesh NoC which shows better behaviors when implementing the median filter on it relative to the 2D mesh based median filter implementation.

## V. Median Filter Implementation on NoC

In this article we used Heracles which is an open source multi core platform written in Verilog with RISC architecture and MIPS core as processing unit [14]. In addition, it is fully parameterized and modular which can be reconfigured and synthesizes into different topologies and size [14]. We used single issue in-order MIPS core with 7 stages pipelined as processing element. Local memory size can be set on a per core basis. This allows both Shared Memory (SM) and Distributed Shared Memory (DSM) implementations. A new topology is constructed by changing some parameters such as, routing algorithm and all routers architecture. In Fig. 5, we show reconstructed 3D mesh router which contains 7 I/O bidirectional channels for Core, Front, Back, East, West, South and North connection.

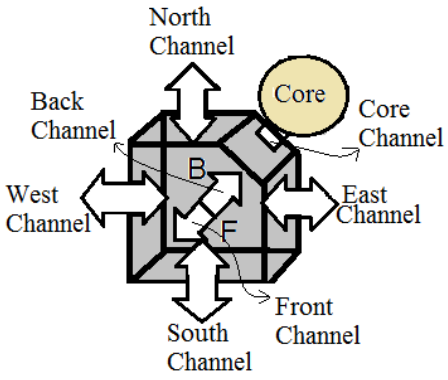


Fig. 5. Reconstructed 3D router with 7 I/O bidirectional channels.

We developed the median filter implementation code in Heracles C programming language. Then we compile these codes to binary MEM files and load them into each core. Also, we wrote median filter as a function unit and divide the tasks between cores. We used Mother-Worker processing methodology. In this case, one core is set to mother core and the other cores are worker. Mother core collects all information of worker cores and writes all output results in own Cache file. Finally, mother core shows the results. All of cores work in parallel mode. In our median filter each worker core processes on multiple rows of corrupted image. With this mechanism the number of execution clock cycles is reduced in compare to other scenarios.

## VI. Experimental Results

We have implemented the median filter on 2D and 3D mesh NoC. The experiments have been performed by Modelsim SE 10.1c that synthesizes Verilog HDL codes and simulates results. For the convenience of multi-core circuit simulation, loading core memory content (even for the mother core) automatically takes place. To do this, all the simulation commands are written inside a Tool Command Language (TCL) file. Also, read commands from the mother core cache memory and writing it as a text file are placed in this file. Furthermore, we changed and modified Heracles multicore hardware and Toolchain codes to show Cache results in a text file and clock cycles of each processing task.

We used some appointed cores of a given platform that we call them "active cores". In first case, we used a 4×4 2D mesh with respectively 1, 4 and 8 active cores. Then we changed our architecture to a 4×2×2 3D mesh. For our subjective and objective analysis, several standard 80×80 pixels gray scale images with a certain percentage of Salt & Pepper noise used which only showed two images. Also, we make some comparison between our results. Fig. 6 shows two corrupted and restored images with NoC based median filter.

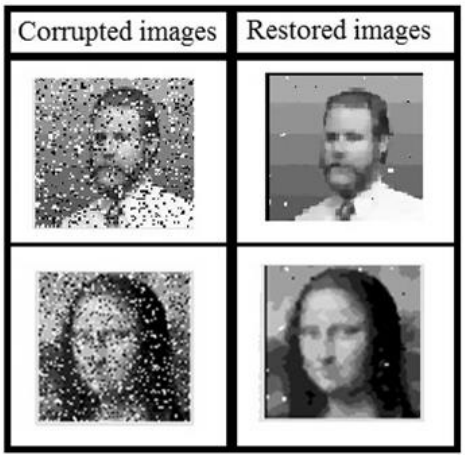


Fig. 6. Corrupted and restored images with NoC based median filter.

Table I shows obtained results and gives a task execution clock cycle comparison between two kinds of NoCs. The results shows that the number of clock cycles for a single core architecture in both of 2D and 3D mesh are the same, but for 4 and 8 core architecture, respectively we have 8.7 percent and 11.8 percent improvement in execution clock cycle count. Also, we guess that increasing the number of core reduces 3D mesh processing clock cycles more than what happens in

2D mesh. Therefore, for multi-core systems that utilize a high number of cores for fast and parallel processing, the use of 3D mesh architecture is highly recommended.

TABLE I. COMPARISON OF PROCESSING CLOCK CYCLE OF TWO METHODS

| Number of used cores | Methods | |
|---|---|---|
| | 2D mesh architecture (4×4 platform) | 3D mesh architecture (4×2×2 platform) |
| 1 | 3e+6 | 3e+6 |
| 4 | 141496 | 129096 |
| 8 | 53128 | 46824 |

## VII. CONCLUSION

In this work, we present an efficient 3D NoC mesh based median filter implementation that is compared with 2D mesh configuration. The implemented median filter is capable of satisfactorily restore the images that corrupted by Salt & Pepper noise, which is a heavy processing task. Also, we developed Heracles design toolkit which contains HDL modules and other tools. In this environment we create our 3D multi-core system. Finally, we synthesis and simulate our architecture in Modelsim SE and compare results of two kinds of 2D and 3D methods. Simulation results shows that implementation of 3D mesh based NoC is achieving less processing clock cycles than 2D mesh based NoC.

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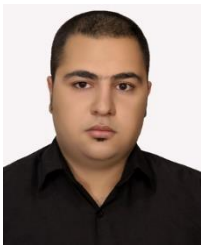

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