FPGA Implementation of Optimized QPSK and OQPSK Using VHDL

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Abstract —This paper proposes a field-programmable gate array (FPGA) architecture of two different modulation schemes, i.e. quadrature phase-shift keying (QPSK) and offset QPSK using hardware description language (HDL) optimized model. It also presents an overview of the FPGA device utilization and performance parameters for both modulation techniques using proposed optimized design. Performance results are provided in terms of the speed of the circuit to show the superiority of the proposed architecture. In this paper, QPSK and OQPSK modulation techniques have been implemented on FPGA using VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) on Xilinx ISE 14.1

Index Terms—FPGA, VHDL, QPSK modulation, OQPSK modulation

I. Introduction

Modulation is a widespread approach in many communication systems to transfer and receive information devoid of any losses through the channel as well as to decimate the size of the antenna under any circumstances of a wireless communication. The technology of wireless communication has become a benchmark amongst the most prevalent technologies in the field of communication today. It is as a result of the proliferation of technology in communication networks facilitated principally at the cellular level of communication as well as wireless information sectors. Such systems require great information rates for reasonable data transmission. A highly common modulation method devised for today`s communication systems is the Quadrature Phase Shift Keying (QPSK), which employs a type of technique called as Phase Shift Keying (PSK). This is mainly due to the uses of digital modulation being evident, such as durability, cost and a simpler reconfiguration when compared with analog. In the modulation technique of Phase Shift Keying, the so called phase varies as per the baseband information while the amplitude and frequency stay unaltered. In QPSK, the technique depicts carrier phase, which gains four discrete, defined states which are utilized to designate groups of two information bits as input as illustrated in Table I. Each of these groups takes only one type of the QPSK states, that is, ±135 °and ±45 °[1].

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Here the very first bit stands for In-phase (I) whereas the second one stands for Quadrature-phase (Q). For the modulation techniques BPSK and QPSK, the BER to SNR ratio are always identical. When we add up two BPSK waves, the QPSK wave is generated. Generally, QPSK has a symbol period of T = 2Tb, whereas for BPSK it is merely 1Tb. The QPSK wave makes use of only half of the necessary bandwidth of the relating BPSK wave that shows a meager throughput when hardware execution is done. In order to conceive a high throughput in the QPSK modulator and to assess the above explanation, equipment usage remains essential. [2].

The organization of this paper is as per the following. Section 2 and Section 3, briefs about the proposed procedure on how to optimize the QPSK and OQPSK. Section 4 demonstrates the design architecture for FPGA and also the full-fledged ModelSim simulation results as well and the conclusions are given in section 5.

II. Optimized QPSK Design (HIGH Throughput QPSK Design)

In this section we shall discuss how optimization of a QPSK transmitter can be done to implement hardware as well as for generating HDL code.

A. Indroduction

This Optimized version of the Transmitter for QPSK shows how designing of Simulink based blocks aiding HDL code can help in the implementation of processing of the baseband of a communication transmitter (Tx). The HDL code can be produced from an entire QPSK based receiver- transmitter chain which in turn is obtained through employment of the HDL based Transmitter along with the HDL based receiver (Rx) given within the Optimized version of QPSK based HDL receiver. On the zenith layer of hierarchy, there lie additives, HDL based Transmitter and sign exceptional measurement. This HDL based Transmitter subsystem has been crafted specifically for HDLtype code era through utilizing hardware pleasant blocks and layout practices [3].

These In- phase (I) and a type of quadrature based (Q) channels are basically produced by the HDL code based Transmitter subsystem which serves as input vector to a Root Raised cosine filter. This subsystem has an output which looks like a hears beat shaped up – sampled symbol. The RRC Filter and the constellation scope

diagram are included in the signal quality measuring subsystem. The purpose of the scope is binary. Both of these holds use for presenting the statistics concerned with the output as well as to compute the MER (Modulation Error Ratio) and EVM (Error Vector Importance) values. Consequent improvement of the EVM can be performed by expanding the fractional bits for these constants present by means of re-sampling this particular RRC filter out for offering a steadfast reaction [4].

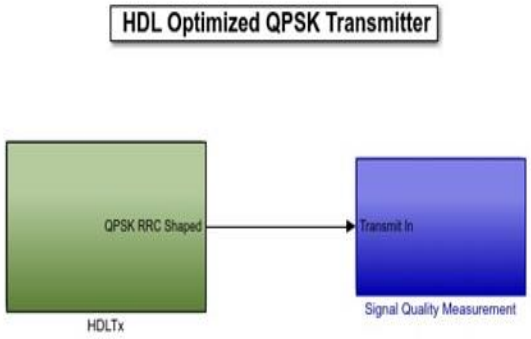

Fig. 1. Block diagram of optimized QPSK transmitter subsystem

B. Components of the HDL Optimized QPSK Transmitter

There are three specific subsystems which are present in the HDL Optimized transmitter. They are as follows:-

1. Data Generation & Packetization Component
2. Symbol Mapping Component
3. Pulse Shaping Component

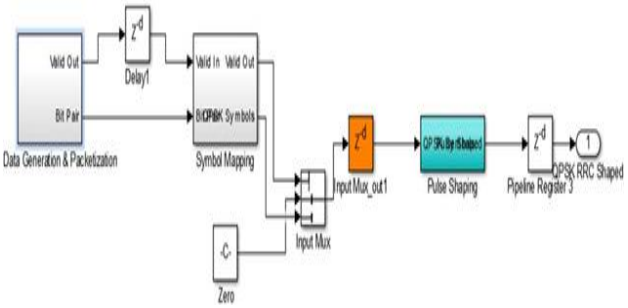

Fig. 2. Connection diagram of internal components of QPSK transmitter subsystem

Data Generation & Packetization: Fig. 2. Illustrate the connection diagram of internal components of QPSK ternsmitter substyetm. Both the Statistics and preamble bits are generated by both the packetizer along with the information source, and these perform the function of packetization along with scrambling. Basically, these packets contain scrambled sources of data which are 174 bits in size and barker code of 26 bit size. The function of a Bit pairing subsystem is to convert input data bit into output of two bits. The Bit pairing subsystem also downsizes rate of pattern by two, fixing a down sample within a manageable route which ensures that the rate of the pattern fits the right direction of signal [5].

Symbol Mapper: Its main function is to map value of input integer [0, 1, 2, 3] to the exact value of complex symbol that is [-1 - 1i,1 + 1i, 1 - 1i, -1 + 1i]. Doing this way of mapping allows only two bits to represent each symbol.

Pulse Shaping: This component makes use of a Root Raised Cosine impulse response and an FIR based interpolation filter, utilizing an up- sampling of four. Here pipelining is done on the filter to make sure that minimization of combinational delay takes place through the whole design [6].

III. Optimized OQPSK Design (High Throughput QPSK Design)

Fig. 3. Illustrate the connection diagram of internal components of OQPSK ternsmitter substyetm. In OQPSK when compared to QPSK, the only difference is that there is an offset after the data packetization blockset. There is a delay after the data generation output [7].

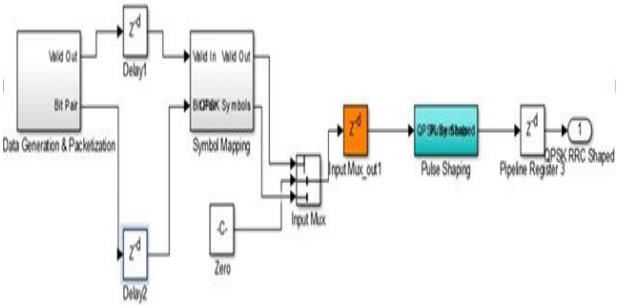

Fig. 3. Connection diagram of internal components of OQPSK transmitter subsystem

IV. Simulation Results

A proposed design for traditional QPSK based modulator can be demonstrated with the help of Verilog based code and this design can be simulated using the Xilinx design suite. The essential perspective behind the simulation of this very basic QPSK modulator is for examining this with the proposed QPSK based modulator in terms of high throughput that is energy usage, area and timing in the FPGA kit. Now VHDL based code synthesis is done from every one of these layouts and they are carefully examined with the help of ModelSim software. The code synthesized is then translated into Register Transfer Level (RTL) schematic diagrams, even as the timing diagram is gained by running the top level code in Xilinx software platform. This simulator now generates the necessary decimal or binary records and then uses analog based signals for devising the required number of waveforms [8].

A. Conventional QPSK Modulator

The Fig. 4. indicates the Register Transfer Level (RTL) schematics acquired with the aid of synthesizing VHDL based code for traditional QPSK based modulator. From the timing diagram of the conventional QPSK based modulator as in Fig. 5, we can see that even or odd information keeps on varying from 00 towards 01 and then eleven towards 10. So this information acquired helps to provide I and Q levels, by multiplying it with a service wave generator. Then these I and Q levels are

introduced to each phase to yield QPSK based signal right here usage of DDS can be observed as well as a 16 stages design to give the result as e cosine wave and sine wave [9]

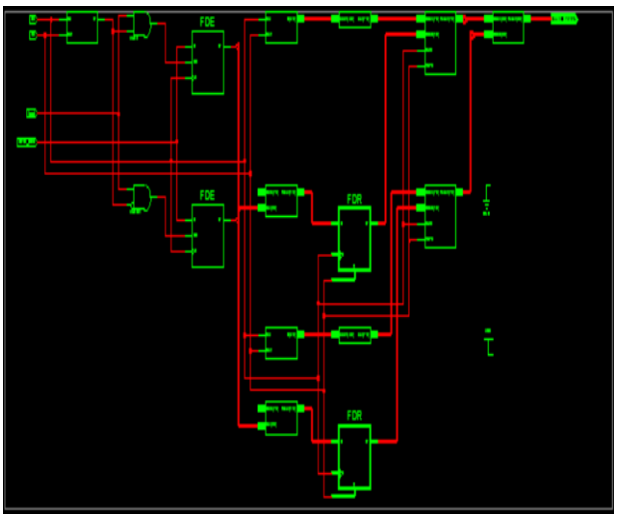

Fig. 4. Top level Register Transfer Level(RTL) for conventional QPSK based modulator

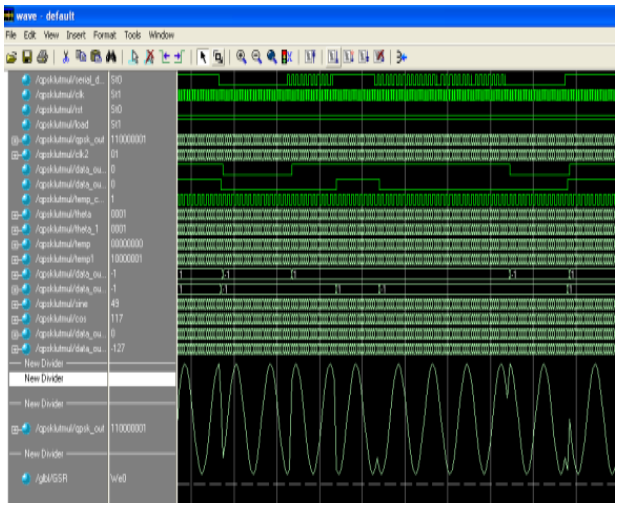

Fig. 5. Simulation for conventional QPSK based modulator

B. Proposed QPSK Modulator

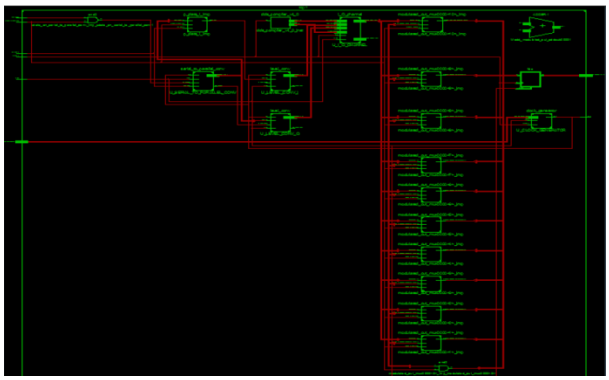

Fig. 6. Top level Register Transfer Level (RTL) Schematics for the proposed QPSK modulator

The Fig. 6 indicates the RTL schematics acquired with the aid of synthesizing VHDL based code for proposed QPSK based modulator. And the timing diagram of the proposed QPSK based modulator as in Fig. 7. In this method, one of the phases requires 0.02µsec and producing one such cycle of the sinusoidal wave needs 1µsec gives you about 50 such samples just by utilizing the up and down accumulator.

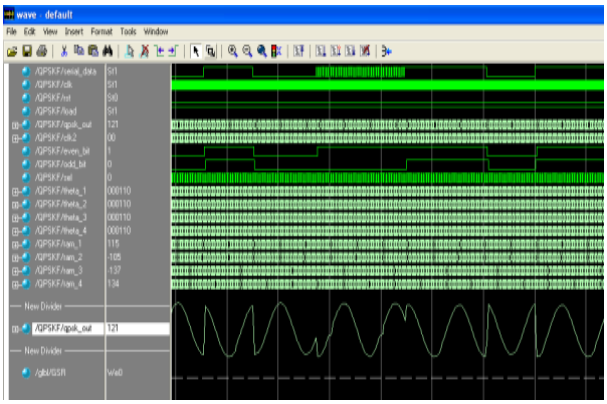

Fig. 7. Simulation for proposed QPSK based modulator

C. Conventional OQPSK Modulator

The Fig. 8. shows the RTL schematics acquired with the aid of synthesizing VHDL based code for traditional OQPSK based modulator. The timing diagram of the conventional OQPSK based modulator is shown in Fig. 9.

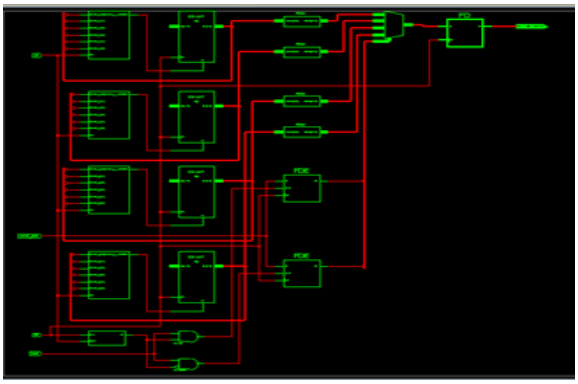

Fig. 8. Top level Register Transfer Level (RTL) Schematics for proposed OQPSK based modulator

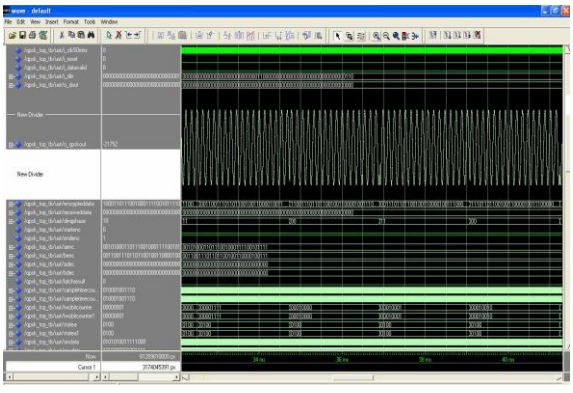

Fig. 9. Simulation for proposed OQPSK based modulator

D. Proposed OQPSK Modulator

The proposed OQPSK modulator is the optimized model of the conventional design acquired by feeding

HDL Code into the system, hence high throughput is achieved. In the proposed design, when comparing to QPSK modulator, there is only an additional delay block which is to be inserted after the Data generation subsystem output as in Fig. 10. The timing diagram of the proposed OQPSK based modulator is shown in Fig. 11.

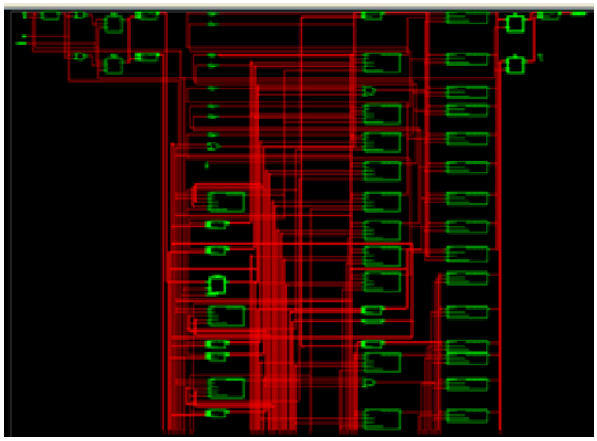

Fig. 10. Top level register transfer level schematics for for proposed OQPSK based Modulator

TABLE I: DEVICE UTILISATION REPORT (XILINX ISE SUITE) FOR THE CONVENTIONAL QPSK MODULATOR DESIGN

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1098	54576	2%
Number of Slice LUTs	1356	27288	4.96%
Number of fully used LUT-FF pairs	831	1623	51.2%
Number of bonded IOBs	36	218	16.51%
Number of BUFG	1	16	6.25%

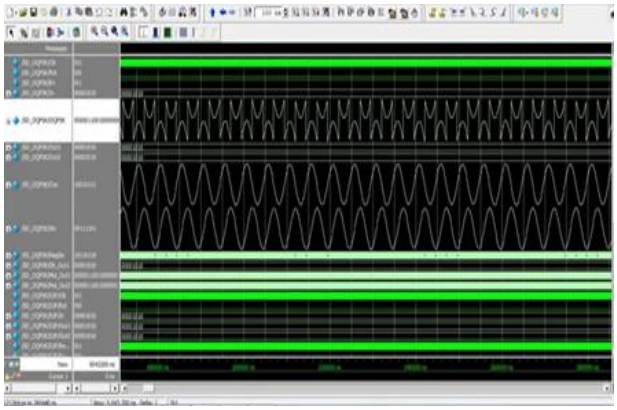

Fig. 11. Simulation for the proposed OQPSK based modulator

The modulator turned into Verilog HDL code, is being applied to Spartan-3E FPGA package with all the above three designs. A synthesis file is generated by the Xilinx synthesis tool, mentioning the parameters utilized by the whole implementation which are show in Table I to Table IV for both QPSK and OQPSK. The performance of the proposed method is compared to conventional method based on the combinational delay and speed of circuit are shown in Table V. From the Table V, It is clearly observed the performance improvement of the proposed method based on both the parameters.

In general, the performance of a circuit entirely depends upon area, circuit delay and speed. The accurate optimization of these parameters will ensure the highest performance of this device. But sometimes one of these will have to be optimized at the cost of another parameter or two.

TABLE II: DEVICE UTILIZATION REPORT (XILINX ISE SUITE) FOR THE PROPOSED QPSK MODULATOR DESIGN

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	105	54576	0.192 %
Number of Slice LUTs	97	27288	0.355%
Number of fully used LUT-FF pairs	74	1623	4.55%
Number of bonded IOBs	58	218	26.6%
Number of BUFG	1	16	6.25%

TABLE III: DEVICE UTILIZATION REPORT (XILINX ISE SUITE) FOR THE CONVENTIONAL OQPSK MODULATOR DESIGN

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	91	54576	0.1667%
Number of Slice LUTs	81	27288	0.296%
Number of fully used LUT-FF pairs	69	1623	4.25%
Number of bonded IOBs	55	218	25.22%
Number of BUFG	1	16	6.25 %

TABLE IV: DEVICE UTILIZATION REPORT (XILINX ISE SUITE) FOR THE PROPOSED OQPSK MODULATOR DESIGN

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	926	54576	1.6967%
Number of Slice LUTs	823	27288	3%
Number of fully used LUT-FF pairs	734	1623	45.22 %
Number of bonded IOBs	42	218	19.26 %
Number of BUFG	1	16	6.25

TABLE V: PERFORMANCE COMPARISON BETWEEN ALL FOUR MODULATORS

Timing Summary	Con. QPSK	Con. OQPSK	Prop. QPSK	Prop. OQPSK
Combinational delay (Minimum Period)	5.272 ns	5.453 ns	5.028 ns	5.216 ns
Speed of Circuit (Operating Frequency)	189.672 MHz	183.385 MHz	198.886 MHz	191.71 MHz

V. CONCLUSIONS

Both the proposed QPSK and OQPSK use a number of functional blocks to optimize the functioning and overall power of the conventional concepts of the QPSK and OQPSK Modulators. From the device utilization reports (area report), it can be seen that the proposed QPSK modulator takes up more area than the conventional QPSK modulator, but from a timing report it is observed

that high speed or throughput is achieved by the proposed QPSK modulator. In case of OQPSK as well, the proposed model occupies more area than the conventional, but operates at a higher throughput when compared to conventional one. From this it is able to conclude that both the proposed models occupy more area, but they work at a higher speed compared to the conventional ones.

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