

The Method of Real-Time Data Weighting Operations of CPLD/FPGA in Measurement Systems

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Abstract—For measurement systems, guaranteeing the accuracy is the primary task and optimizing resources has strong connection with low power consumption and low cost. There is a need for smooth filtering, median filtering and some other data processing in Complex Programmable Logic Device or Field—Programmable Gate Array design of measurement systems. And the weighted arithmetic is indispensable for filtering. Combined with the characteristics of data acquisition in measurement systems, a new real-time weighted method is put forward. This method does not need to call IP core and built-in CPU. Two data registers with different bits are designed in Complex Programmable Logic Device or Field — Programmable Gate Array. Combining with the addition and shift operation of the input data with the addition and shift operation of quotient together to form the new weighted division data, this method owns the advantages of good real-time ability and high accuracy compared with the conventional division operations. And it can be used in the Complex Programmable Logic Devices without IP core, as well as in low power consumption Field—Programmable Gate Arrays. This method achieves the goal of utilizing resources according to the function realization of the measurement systems. To acquire the same function with the traditional design pattern, the feasibility and effectiveness of the method described in this article are verified through designing five-order smoothing filter test. This method has been used in a project, which proves that the method is reliable, efficient and stable in practical application.

Index Terms—Measurement systems, division operations, data acquisition, CPLD/FPGA, IP core, geophysical instruments, data weighting

I. INTRODUCTION

Data acquisition and data processing are key units in measurement systems commonly. With the development and progress of technology, high-precision and high-speed data acquisition technology has been widely used [1]-[4]. As an essential part in the measurement systems, data preprocessing is critical. Therefore, Complex Programmable Logic Device or Field — Programmable Gate

Array (CPLD/FPGA) is in extensive use as typical representation of parallel processing [2], [3].

Addition and division units are the basic preprocessing modules in measurement systems [2], [4]-[6]. Data preprocessing usually needs decimation filtering, low-pass digital filtering and some other filtering operations. In data preprocessing, addition and division operations are the most important units, whose computing speed, performance and power consumption, especially the real-time ability, will affect the overall performance of the whole measurement systems [6]. Compared with other operations, addition and division operations are complex and with low efficiency, so researches on parallel processing devices(e.g. CPLD/FPGA) are rare [2], [3]. However, it cannot be ignored that addition and division operations of data weighting can affect the overall performance of the measurement systems easily without enough attention [7]-[8].

Addition and division operations in data weighting, especially the division operations, generally have three implementation methods in programmable logic chips: 1) The kernel in the FPGA, such as the built-in ARM kernel produced by Xilinx company, can achieve these functions; 2) Intelligence Property core (IP core), some FPGAs have division IP core; 3) Direct shift of internal logic, and the divisor is a power of 2. These three ways have their corresponding faults for measurement systems [5]-[14]. Therefore, for the problems existing in data preprocessing, a real-time addition and division operating implementation method is put forward based on CPLD/FPGA which without IP core. This method can realize smooth filtering, median filtering and other preprocessing operations, and satisfy the requirement for cost, power consumption and resource utilizations of measurement systems. And this method can be applied to other data processing systems, high-precision data acquisition systems (e.g. geophysical instruments) and high-speed data acquisition systems to optimize the design of data processing systems.

II. DATA WEIGHTING PROBLEMS IN MEASUREMENT SYSTEMS

A. Basic Model of Data Flow and Weighting in Measurement System

In measurement systems, a variety of sensors, such as electrodes, measuring pens and other various waveform

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sensors are used for geological exploration, detecting natural fields under strata, seismic waves and electromagnetic waves produced by controllable source, or measuring the amplitude, phase and frequency features of the communication signals or other high-speed signals [5]. The signals of high-precision measurement systems are very weak generally, which need further improvement of the SNDR features to make up for the front-end signal loss and high-speed measurement systems also need to get higher SNDR for accurate data acquisition. The data acquisition and preprocessing module diagram of the measurement systems is shown in Fig. 1, [1], [6].

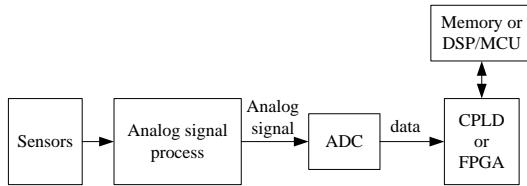


Fig. 1. The data acquisition and preprocessing module

The analog signals after conditioning are sampled to get digital signals in ADC. And then digital signals will be sent to CPLD or FPGA for integrating interface protocols and data preprocessing. The data after preprocessing will be sent to storage chips or for further processing by CPLD or FPGA.

Data preprocessing need to promote the quantization error, reduce the nonlinear error and improve accuracy for providing effective information in further procedure [9]. In measurement system, preprocessing unit needs to judge whether the data acquired in real time is valid or not. If the data is effective, collection and preservation will be done. Or the current data will be abandoned to figure out a method to collect effective data. So there commands more importance on real-time data preprocessing. As an important part of data preprocessing in measurement system, the real-time performance of data weighting directly determines the real-time ability of data preprocessing.

Weighted arithmetic in CPLD or FPGA usually will be needed to be synchronized or real-time to meet the requirements of some special applications[10]. Or it would be difficult to achieve the effective information to make the products meet the needs of customers.

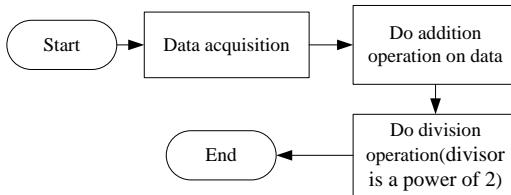


Fig. 2. Data acquisition interface in geophysical instruments

B. Conventional Addition and Division Methods and Their Real-Time Problems Existed

There are several ways for weighting implementation in CPLD/FPGA: 1) Division operation is implemented in CPLD directly, whose divisor is a power of 2. The

precision loss greatly, So it is difficult to achieve high-precision division, and the operation implementation flow chart is shown as Fig. 2; 2) The FPGA with divider can realize the weighted arithmetic division operation with bad real-time ability [4]-[8].

Only high-frequency clock can be used to realize division generally, and then FIFO interface is to implement the data transmission. The accuracy has a strong correlation with the precision of divider. If there is no divider to be designed, the divider in CPLD is unable to realize high-precision operation, which is shown in Fig. 3.

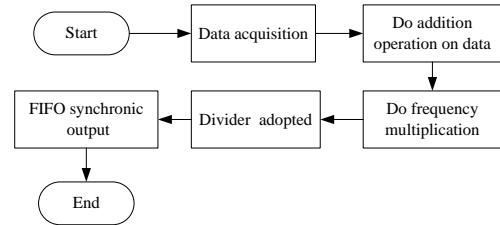


Fig. 3. The weighted arithmetic with divider

As shown in Fig. 3, we can choose to wait at the same frequency, or accomplish division operation using high frequency in the FPGA, but there are some certain restrictions [7].

Weighted arithmetic is usually used in the high-speed data acquisition and processing, so there is a high demand on real-time ability, which largely limits the promotion of the performance [6]. And for the CPLD or FPGA without build-in divider, it will consume a lot of resources to realize weighted arithmetic, affect calculation precision and bring the limitation on calculation.

As shown in Fig. 2, the division can be completed in one clock cycle based on the shift divisor of 2. However, this division is limited by the divisor, which must be an integral multiple of 2. As shown in Fig. 3, conventional method of the weighting arithmetic can only realize weak real-time function to some extent. When there is a need for addition operation, each data should be output completely. And in the next clock cycle, the addition will be realized. Frequency doubling clock is applied on IP core to accomplish the division in weighting. All the processes needs at least 2 minutes, including data input and data output. And it will also have certain clock delay due to the complexity of the division for the division IP core, so the real-time ability cannot be completely implemented. In some FPGAs without division IP core and CPLDs, only the division based on the shift divisor of 2 can be implemented, which leads unacceptable error for the measurement system. And the weighting data is worse than the original data probably.

III. REAL-TIME OPERATION IMPLEMENTATION

A. The Weighted Arithmetic Implementation Model

With the progress and development of technology and electronic industry, the advantages of the programmable digital logic devices FPGA and CPLD are becoming

more and more outstanding, and the majority of the measurement systems adopt FPGA or CPLD [11]. Many measurement systems need to adopt weighted arithmetic to improve measuring accuracy and to extract effective information. The real-time weighted arithmetic realization method proposed is based on the use of FPGA without IP core or CPLD.

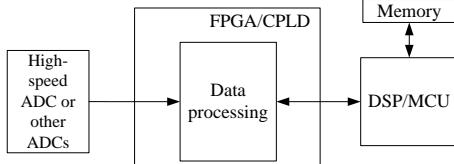


Fig. 4. The weighted arithmetic implementation model

As shown in Fig. 4, the arrows on the diagram indicate the starting point and the flow of the data. The data transfer from the ADC, and will be received in programmable digital logic device FPGA or CPLD. Then the data calculation will be implemented and completed in the FPGA or CPLD. Then the processed data is sent to DSP and MCU through the corresponding data interface for storage or further processing.

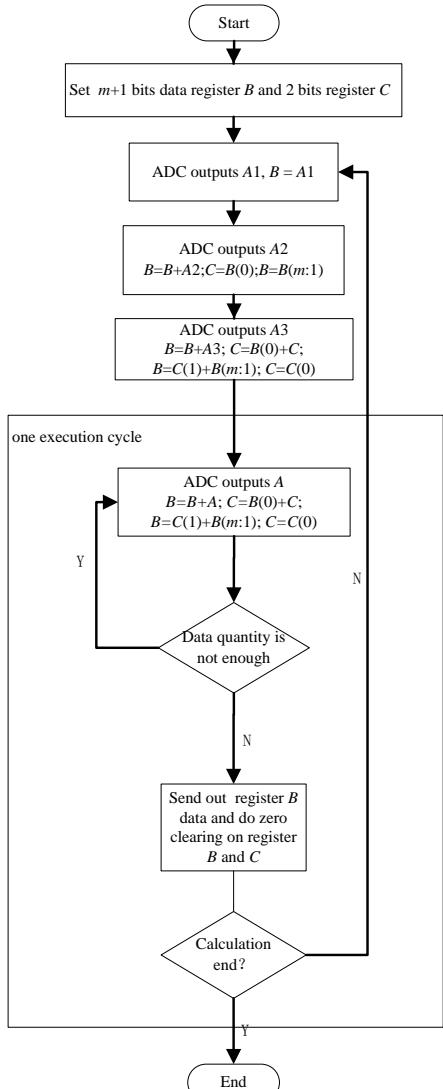


Fig. 5. Weighted arithmetic implementation flow chart

B. The Procedure of Weighted Arithmetic Implementation in CPLD/FPGA

As shown in Fig. 1, the hardware sensors collect electrical signal, which is sent to ADC after the signal conditioning module. After digital-to-analog conversation in ADC, signals will be delivered to FPGA/CPLD. Signals after preprocessing by FPGA/CPLD are sent for storage or for further processing in center processor. Software mainly consists of control software and algorithm software. Control software starts the ADC data acquisition and conditioning module of control signals. Algorithm software mainly is realized in FPGA/CPLD to accomplish the addition and division operation of high-speed acquisition data, whose procedure is shown in Fig. 5.

- a) Binary data A is output successively from ADC. A consists of A_1, A_2, \dots, A_n and is with m bits. Set $m+1$ bits register B and 2 bits register C in FPGA or CPLD;
- b) Assign A_1 to B according to $B = A_1$. If the left data has more bits than the right register of this equation, the left register zero-pads automatically;
- c) When ADC outputs A_2 , then store $B + A_2$ register B according to $B = B + A_2$;
- d) Assign the last bit data $B(0)$ of register B to C according to $C = B(0)$; store the first high m bits $B(m:1)$ of register B to B according to $B = B(m:1)$;
- e) When ADC outputs A_3 , store $B + A_3$ to B according to $B = B + A_3$;
- f) Select the lowest bit of register B data $B(0)$, do $B + C(0)$ according to $C = B + C(0)$; store the first high m bits $B(m:1)$ of register B to B according to $B = B(m:1)$;
- g) Store the high bits of register C data $C(1) + B$ to B according to $B = C(1) + B$; store the low bits of Register C data $C(0)$ to C according to $C = C(0)$;
- h) When the next output of ADC data A belongs to A_4, A_5, \dots, A_n then perform the calculation of $B = B + A$;
- i) Select the lowest bit of register B data $B(0)$, execute $C = B(0) + C$; store the first high m bits $B(m:1)$ of register B to B according to $B = B(m:1)$;
- j) Store the high bits of register C data $C(1) + B$ to B according to $B = C(1) + B$; store the low bits of register C data $C(0)$ to C according to $C = C(0)$;
- k) If the data quantity of addition and division operation is not enough, then return to step h). If the data quantity of addition and division operation is enough, then send out the register B data and do zero clearing on register B and C . If there is a need to continue the calculation, return to step b). If the calculation is to end, then do the next step;

l) End all the operations; do zero clearing to the whole registers; terminate the addition and division operation; where data A is with m bits and consists of A_1, A_2, \dots, A_n ; B is the $m+1$ bits data register; C is the 2 bits data register.

C. The Weighted Arithmetic Implementation in CPLD/FPGA

In realizing a measurement system, 14bit 400MSPS ADS5474 produced by TI company is adopted as ADC, whose sampling rate is 400MHz [15]. The actual sampling rate is decided by extraction rate. XO2-7000HC-4TG144 produced by Lattice company is used as the programmable logic digital device, in which the

corresponding divider does not exist [16]. The implementation of the module is shown as Fig. 6.

In Fig. 6, we can know that rst_n : active-low reset; os_start : start signal of measuring the output data; os_adc_clk : clock, has the same frequency with sampling rate; os_adc_in : measuring data input; filter_num : weighted parameters; os_pdn : power down control signal; os_adc_out : the output data of the measuring data after weighting; out_sig : output valid signal.

In Fig. 6, os_adc_clk is input signal of 400MHz clock. filter_num is with 7bits, which means the weighting coefficient can range from 0 to $2^7 - 1$. When the os_start is valid, weighted arithmetic, out_sig indicates the output signal after weighting.

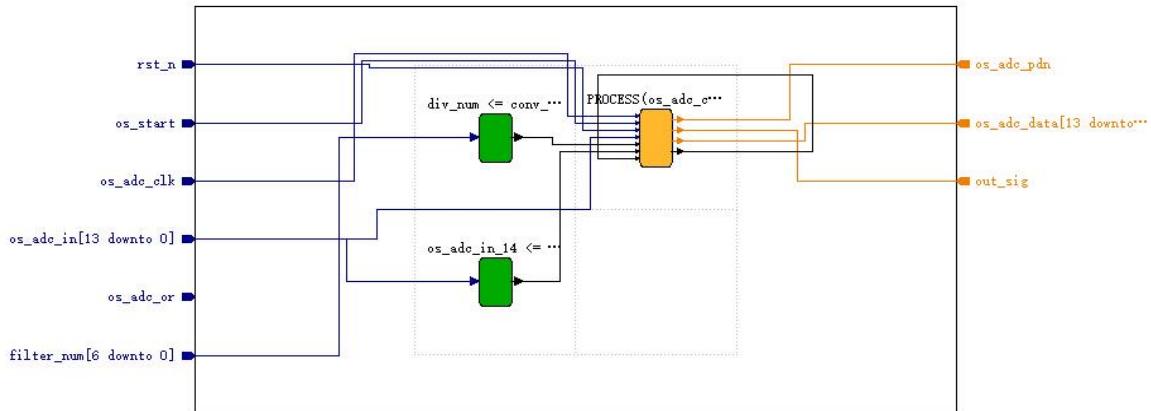


Fig. 6. Weighted arithmetic implementation

The Fig. 7 shows that $\text{os_adc_data_buf_add}$ is the 14+1bit data register and the inner 2bit data register is hidden. 2bit data register is labeled as OS_ADC_DATA_C.

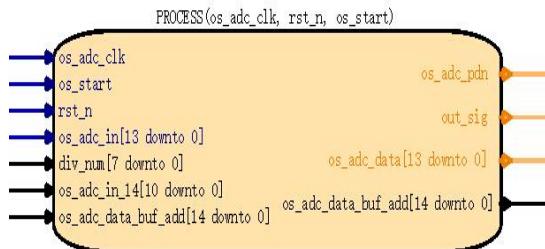


Fig. 7. The inner structure of weighted arithmetic

In the design, the data accuracy loss of one time weighted arithmetic is less than 1bit, which means that if there are x ADC output data to be weighted, the loss is less than $1/x$. Compared with traditional algorithm, the accuracy loss is little.

IV. TEST RESULTS AND PERFORMANCE COMPARISON

A. Output Data Test (Data Acquisition)

In practical testing, signal generator is used to generate 12MHZ sine wave signal, which is collected by high-speed ADC chip ADS5474 [15]. Five-order smoothing filter is designed in XO2-7000HC-4TG144, through which the data is compared with the original data in time domain and frequency domain respectively [16].

The five-order smoothing filter is realized in XO2-7000HC-4TG144 as follows:

- 1) Set up a data register to record the data eliminated in five-order weighted data;
- 2) When a new data is added, minus the data which should be eliminated;
- 3) Design five-order weighted module to complete the smoothing filter.

Fig. 8 is the data acquisition sequence diagram. Fig. 9 is the data after five-order smooth filtering in time domain. Fig. 10 is the data of Fig. 8 in frequency domain. And Fig. 11 is the data of Fig. 9 after five-order smooth filtering in frequency domain. SNDR and ENOB are obtained by MATLAB analysis.

The Fig. 8 is with more sharp peaks and troughs, higher peak-to-peak value, better high-frequency properties, as well as poor anti-interference ability in the time domain. However, the waveform in Fig. 9 is more smooth due to the weighting playing a positive role in smoothing the singular data to suppress the high-frequency interference, which means the weighting bringing with good smooth filtering function. So this method is effective in real-time weighting in CPLD/FPGA.

After five-order smooth filtering, SNDR and ENOB have improved greatly in frequency domain. The notch filters at 80MHz and 160MHz prove the validity of smooth filtering of five-order weighted arithmetic, which

can be seen in Fig. 11. SNDR increases from 58.27dB to 58.27dB and ENOB improves from 9.4bits to 10.7bits through five-order smooth filtering, which can be

calculated and verified through theory. The test proves the validity of the weighted arithmetic implementation proposed in this paper.

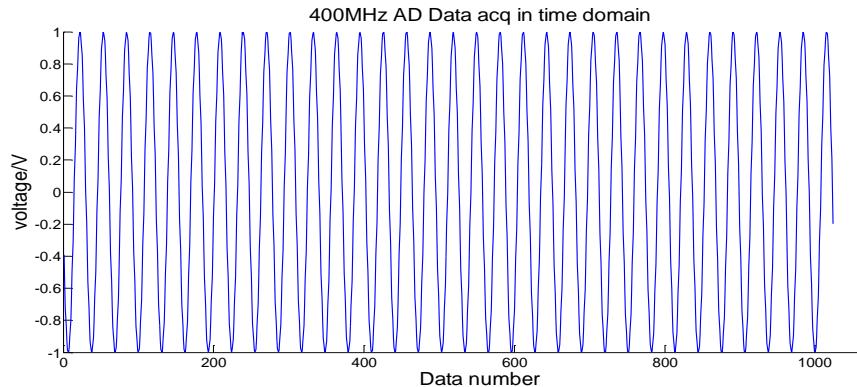


Fig. 8. Data acquired in time domain

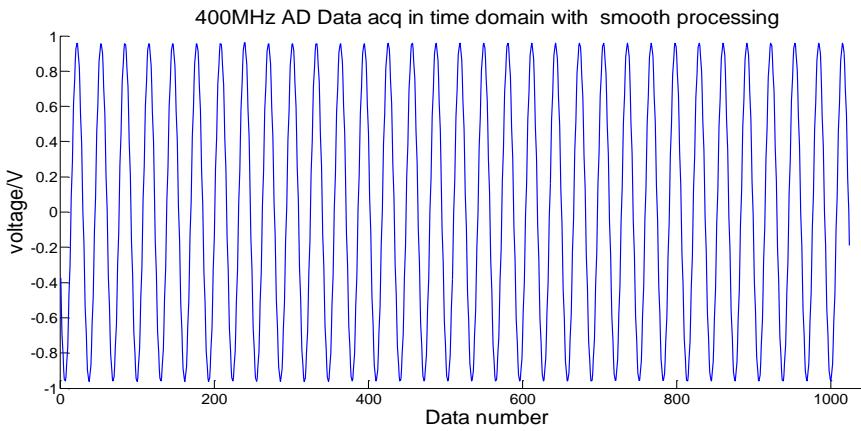


Fig. 9. Data acquired after five-order smooth filtering in time domain

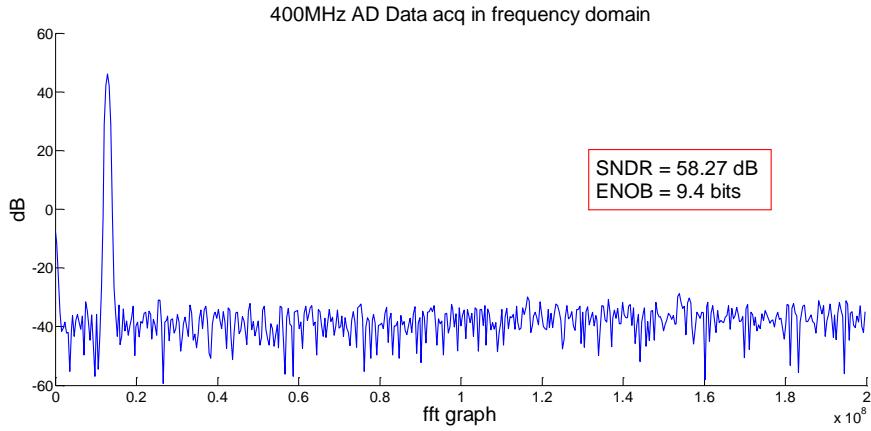


Fig. 10. Data acquired in frequency domain

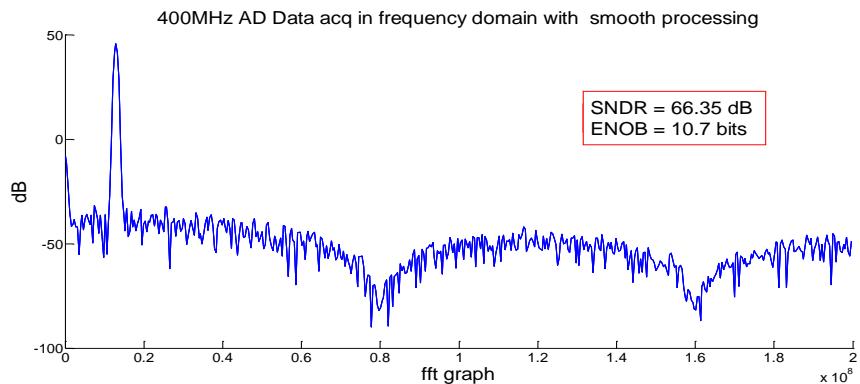


Fig. 11. Data acquired after five-order smooth filtering in frequency domain

In practical engineering, the higher the sampling rate, the more difficult the traditional weighting method achieves the real-time calculation. Due to the increase of data quantity and the frequency of multiplier, the rate of calculation is limited. So the higher the working frequency, the more superior the proposed method is compared with traditional methods. With bigger weighting series, data obtained is more smooth and with better interference suppression performance. To achieve better smoothing effect, white noise or accidental high-

frequency interference suppression is needed. The burr can be eliminated better by increasing weighting series in measurement system.

B. Performance Comparison

The main contrast object of method proposed with traditional weighted arithmetic is realized in CPLD/FPGA. This method has many advantages, which are shown in Table I.

TABLE I: COMPARISON BETWEEN THE PROPOSED METHOD AND TRADITIONAL METHOD

	The method proposed	Traditional method	
		with divider or build-in processor	no divider
1	Resource utilization	2 data registers	1 divider +1 PLL + 2 data registers
2	Power consumption	almost none	large
3	Cost	almost none	high
4	Accuracy	$1/x$	$>1/x$
5	Real-time ability	1 clock	more than 3 clocks
6	Limitations	few in data preprocessing	more than 2 clocks
7	Designation complexity	simple	many arithmetic is not available simple

Table I shows that the method proposed has great advantage on real-time ability and resource utilization, compared with traditional methods, IP with divider or CPLD/FPGA with build-in processors. It is clear that the maximum error is the inverse of weighting, which improves the calculation accuracy greatly. Compared with IP core with divider or CPLD/FPGA with build-in processors, high precision is the most outstanding advantage of this method. That the traditional method realizing the smooth filtering in CPLD will be counterproductive. In the low power consumption and low cost CPLD design, IP core with divider or embedded ARM processor is not accepted.

V. CONCLUSION

With the rapid development of electronic industry, as important tools of industrial design and project implementation, measurement systems play very important roles in measuring fields. As the final measuring execution systems, its precision, real-time ability, designation complexity, cost and resources need comprehensive consideration. For weighted arithmetic, the designers employ division IP core or FPGA with embedded ARM processor to realize considering with accuracy issues, which usually consumes a large amount of DSP resources of FPGA or needs to set up complex embedded environment, and is with weak real-time performance.

Aiming at solving the above problems, combined with the logic feature of CPLD/FPGA, a method of direct weighted arithmetic is put forward in the process of data acquisition and data preprocessing in measurement systems to achieve the excellent real-time ability of weighted arithmetic based on CPLD/FPGA. And this method uses data register to accomplish directly shift and addition operation and needs CPLD/FPGA to achieve low power consumption and high real-time division

The real-time weighted arithmetic implementation method proposed is based on CPLD/FPGA, so combined with 400MSPS high-speed data acquisition of the actual project, the smoothing filtering is done in CPLD/FPGA. And the filtering utilizes weighted algorithm to meet the requirements of real time and high accuracy, which improves the SNDR and effective digits of measurement system effectively. The method proves to be effective and feasible

Compared with conventional methods, this method saves the cost and resources, improves the calculation accuracy and real-time performance, therefore there are great improvements on the power consumption, cost, resource utilization and the designation complexity of measurement systems. The method proposed is not only successfully applied in the high-speed data acquisition system, but also fully used in a high-precision data acquisition instrument. The method proposed can also be employed in geophysical instruments to realize data preprocessing, which could effectively improve the resource utilization and reliability of geophysical instruments.

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REFERENCES

- [1] E. O. Doebelin, Measurement Systems - Application and Design, Fourth Edition, McGraw-Hill International Editors, Mechanical Engineering Series, 1976.
- [2] P. A. N. Ming and X. U. Yong, "FPGA design and implementation of add-subtraction alternate algorithm division," *Control & Automation*, vol. 24, pp. 141-143, Feb. 2008.
- [3] F. B. Yan, J. X. Liu, et al., "Study of the way to firmware program upgrade in FPGA reconfiguration of distributed geophysical instruments," *Sensors & Transducers*, vol. 172, no. 6, pp. 130-138, Jun. 2014.
- [4] R. S. Bird, "A simple division-free algorithm for computing determinants," *Information Processing Letters*, vol. 111, pp. 1072-1074, 2011.
- [5] Q. Hong, Z. W. Zhao, and M. He, "Design and implementation of high-performance float-point division and square root," *Computer Engineering*, vol. 39, no. 12, pp. 264-268, Dec. 2013.
- [6] L. F. Chen and G. Guo, "Nearest neighbor classification of categorical data by attributes weighting," *Expert Systems with Applications*, vol. 42, pp. 3142-3149, 2015.
- [7] X. Ye, H. Zhang, D. Pi, et al., "Design of integer divider with adjustable precision based on verilog," *Modern Electronics Technique*, vol. 290, pp. 146-147, Mar. 2009.
- [8] H. C. Tang, "Simulated division with approximate factoring for the multiple recursive generator with both unrestricted multiplier and non-mersenne prime modulus," *Computers & Mathematics with Applications*, vol. 46, pp. 1173-1181, 2003.
- [9] R. I. C. C. Francis, "Data weighting in statistical fisheries stock assessment models," *Canadian Journal of Fisheries & Aquatic Sciences*, vol. 68, pp. 1124-1138, 2011.
- [10] F. B. Yan, J. X. Liu, et al., "The key signals integrity simulation and implementation of portable processing terminal in the special environment," *Sensors & Transducers Journal*, vol. 181, no. 10, pp. 146-154, Oct. 2014.
- [11] H. L. Wei and N. A. M. Isa, "Adaptive division of labor particle swarm optimization," *Expert Systems with Applications*, 2015.
- [12] D. Zhou and J. Wang, "Design of a 32-bit divider based on FPGA," *Informatization Research*, vol. 36, No. 3, pp. 26-28, Mar. 2010.
- [13] X. Hu, X. Liao, and C. Huang, "Data weighting and solution assessment in combination," *Journal of Geodesy*, vol. 73, pp. 391-397, 1999.
- [14] F. Yan, J. Liu, and Y. Su, "A method of serial data clock domain crossing transmission in geophysical instruments," *Journal of Communications*, vol. 10, no. 6, pp. 429-434, 2015.
- [15] Texas Instruments Inc., ADS5474 14-Bit, 400-MSPS Analog-to-Digital Converter, Aug. 2008.
- [16] Lattice Semiconductor Corp., MachXO2 Family Data Sheet Introduction, Data Sheet DS1035, Sept. 2014.



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