

A Method of Serial Data Clock Domain Crossing Transmission in Geophysical Instruments

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Abstract—Power-consumption reduction, resource optimization and cost reduction are inevitable on geophysical instrument design. We propose a new method for serial data clock domain crossing (CDC) transmission to solve the resource utilization problem of data acquisition interface in geophysical instrument design, combining with the use of digital programmable logic chip FPGA/CPLD. This method changes the usage mode of several simple serial-to-parallel and parallel-to-serial converting registers in original design to convert the CDC serial data instead of the traditional FIFO transfer way, which saves FIFO chips or FIFO modules in programmable logic chip resources fundamentally and can realize the same function as traditional design mode. Through long time verification in practical engineering, the method we proposed can be proved to be with reliability, effectiveness and stable operation.

Index Terms—FPGA/CPLD, Sigma-Delta ADC, Geophysical Instruments, clock domain crossing (CDC), data acquisition, Serial bus, FIFO

I. INTRODUCTION

As an indispensable part of geophysical instruments, data acquisition plays a crucial role [1]. However, geophysical exploration signals are commonly so weak that there is a need for high-precision acquisition of these signals. In that case, Sigma-Delta ADC is adopted for high-resolution data acquisition to achieve geological information effectively for better data analysis [1], [2].

In many geophysical instruments, Sigma-Delta ADCs generally uses serial interfaces. Data received from ADCs will be sent to low-power-consumption processors, which adopt the serial interfaces with different clock frequencies to receive data as well [3]. In this case, many instruments usually adopt FIFO mode to do CDC data interactive transmission to ensure seamless data receiving [2]-[4].

Special FIFO chips or programmable digital logic chip FPGA or CPLD chips will be used as FIFO receiver

generally. The use of these chips increases the instruments' cost and the volume. However, these chips are inevitably adopted in geophysical instruments, which bring great power consumption because of the resource occupancy of FIFO and resource utilization problem [5].

Therefore, we propose a method, which can adapt CDC serial data interaction, for the data acquisition problem of geophysical instruments to meet the low-cost, low-power-consumption and small-size requirements of those instruments. The circuit realization of this method can also be applied in other serial data interactive situations to achieve the purpose of the design optimization.

II. SERIAL CDC DATA ACQUISITION PROBLEM

A. Base Model of Geophysical Instruments

In geophysical instruments, a variety of sensors, such as electrode, magnetic field sensors and other kinds of waveform sensors will be adopted to do geological exploration to detect seismic waves and electromagnetic waves produced by natural field or controllable sources in stratum. Under many circumstances, signals received by these sensors are so weak that low-noise operational amplifiers are required to amplify these signals, especially the signals generated by natural field. Because signals are with low frequency, we do low-pass filter processing to signals that are with higher frequency than useful signals, and mainly eliminate 50Hz or 60Hz power-frequency signals, as well as other high-frequency signals [1]-[4].

Through conditioning, the analog signals go into the interface of high-resolution of Sigma-Delta ADC for analog-to-digital conversion to facilitate the subsequent processing. 24-bit ADC, whose interface uses serial bus with unique format, is commonly adopted. The front-end data format and frequency relate to the front-end sampling frequency and the included analog-to-digital converting channel number of Sigma-Delta ADC. The clock rate generally ranges from several hundred Hz to several million Hz. Data formats own channel identifiable bit, data bits and start stop bit, and because the channels are not identical, the data are same as well [6].

As show in Fig. 1, in the back-end FPGA+DSP+MCU, FPGA or CPLD receive data, and then pass the data to DSP or MCU to do comprehensive processing [7].

Manuscript received March 27, 2015; revised June 25, 2015.

This work was supported by the National Science and Technology Infrastructure Funds of China(2013FY110800), National Natural Science Funds of China(41174103), National High Technology Research and Development Program of China (863 Program)(2014AA06A615), the Fundamental Research Funds for the Central Universities of Central South University(2015zzts065).

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doi:10.12720/jcm.10.6.429-434

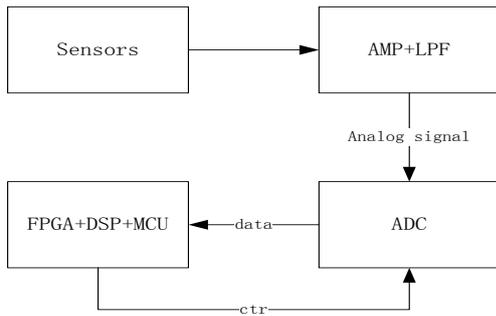


Fig. 1. Block diagram of Geophysical Instruments

B. CDC Serial Data Interaction Problem

Sigma-Delta ADC, such as ADCs produced by Asahi Kasei Microdevices located in Japan and Analog Devices, employs serial interface. Only sampling chips with high-rate single channel use the parallel interface. Geophysical

instruments usually adopt distributed design and single chip includes multi-channel ADCs to realize the data acquisition.

As shown in Fig. 2, under the control of serial clock and synchronizing signal of the data, 24-bit data is output from the data channel sequentially. Start and stop clock exists between channel data, and if this data format is input into the data processor, it will bring great burden on the processor [8]-[9]. Therefore, these data need to be rearranged for data transmission under high-frequency clock. The rearrangement should be designed to be in favor of digital signal processor receiving data, digital signal processing, resource utilization and the overall low-power consumption of the instrument.

Therefore, how to transmit data reasonably as well as to save transmission resources to an extreme need each geophysical instrument designer to consider, when facing the problem.

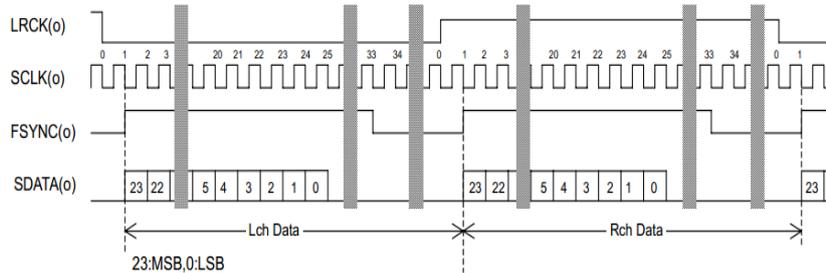


Fig. 2. ADC interface timing diagram[8]

C. The Conventional CDC Serial Data Transmission Model

As shown in Fig. 3, serial data are converted to parallel data first. And then the transformed data are sent to FIFO, with which CDC data conversion will be done. Finally, parallel-to-serial conversation of the FIFO output data are done and the analysis and process of the subsequent digital signal come to an end.

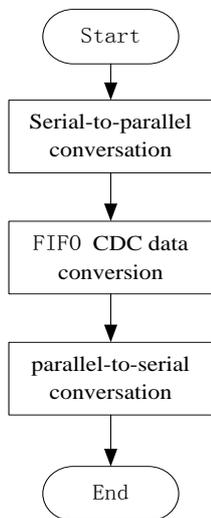


Fig. 3. The process of the data acquisition in geophysical instrument interface

FIFO block diagram is shown as Fig. 4, which can be generated by special chip or programmable logic chip FPGA or CPLD [10]-[13]. FIFO resources contain RAM with a certain depth to storage data. FIFO width equals to data width. When it comes to actual use, the data width is the multiplication of ADC channel number and ADC resolution, adding read and write clock, reset, read and write enable signal, read and write sign signal [6].

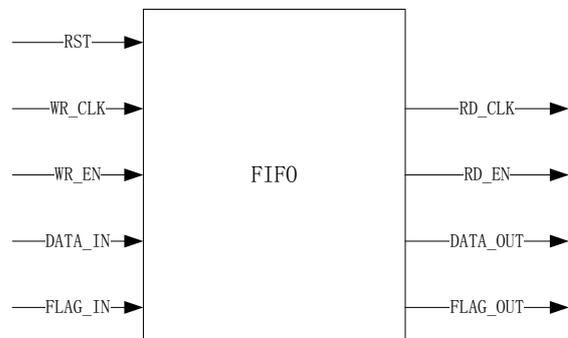


Fig. 4. FIFO block diagram

When receiving and sending data in Sigma-Delta ADC, the conversion between serial data and parallel data under certain timing control is done. Put serial data into a parallel register for receiving data, and the data in parallel register will be output bit by bit while sending data.

III. CDC SERIAL DATA TRANSMISSION METHOD

A. CDC Serial Data Transmission Model

With the development and advancement of science, technology and electronics industry, the advantage of programmable digital logic devices FPGAs or CPLDs is becoming more and more outstanding, and a majority of geophysical instruments have employed digital programmable logic devices FPGAs or CPLDs[11]. So the implementation of the CDC serial data transmission method proposed is based on the use of programmable digital logic devices FPGAs or CPLDs.

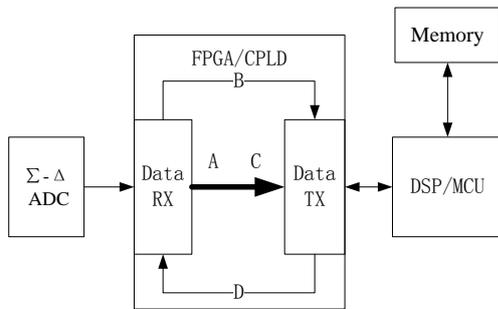


Fig. 5. A new method of data transmission

As shown in Fig. 5, arrows indicate the starting point and the flow direction of data. New CDC data transmission begins at Delta-Sigma ADC. The realization of data receiving is in the FPGA or CPLD. In the process of data receiving, we accomplish data serial-to-parallel conversation under the control of ADC clock. Then we convert the parallel data to serial data under the control of DSP or MCU interface clock. In the data transmission process, we only add two data serial-to-parallel and parallel-to-serial conversion registers and two 1-bit registers, which do data conversion directly without other registers engaging, based on original receiving timing and sending timing.

B. CDC Serial Data Transmission Process

A series of steps needed for CDC serial data transmission is shown in Fig. 6.

The realization of CDC serial data transmission in geophysical instruments is through the following steps.

Step 1: Set a register A with enough digits, and set A to be 0 in the FPGA/CPLD data receiving module;

Step 2: Set a 1-bit signal register B in FPGA/CPLD data receiving module and the initial value of B is 0. The function of B is to let data transmission module in FPGA/CPLD judge whether to send data or not;

Step 3: Set a register C owning the same bits wide with the register located in data receiving module in data transmission module of FPGA/CPLD. C will be used to receive the data of register A. And set a 1-bit signal register D. D is used to send frame data receiving complete signal to data receiving module. And the initial values of C and D are 0;

Step 4: Take advantage of the serial interface clock of Delta-Sigma ADC in the receiving module of

FPGA/CPLD. The clock of data transmission or serial interface in storage module is the same in data processing module and data transmission module;

Step 5: The data receiving module in FPGA/CPLD receives serial data transmitted by Delta-Sigma ADC serial interface under its clock domain. The receiving data will be stored in register A sequentially once 1bit;

Step 6: If the register A is just full after the receiving module in FPGA/CPLD receives a frame serial data from Delta-Sigma ADC interface, set register B to 1;

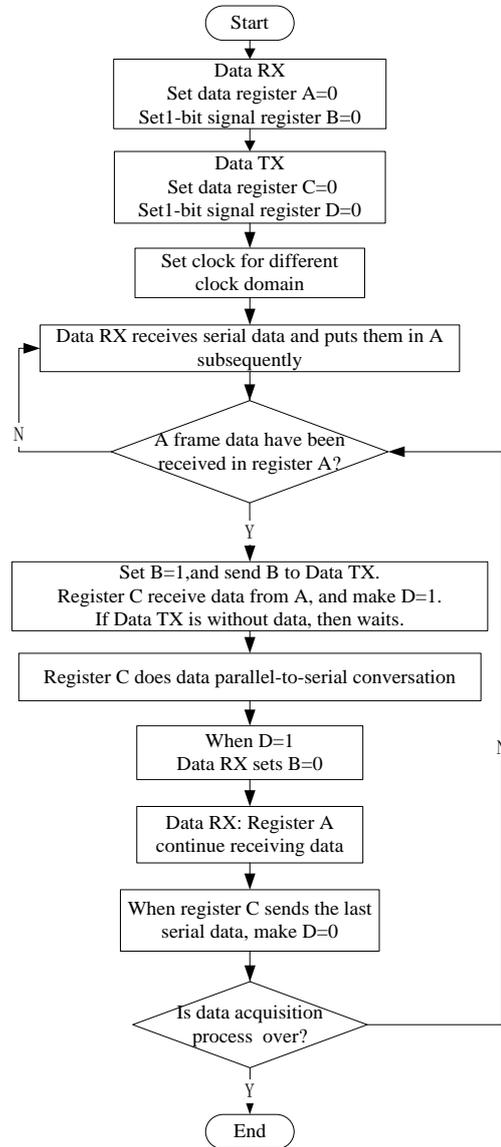


Fig. 6. CDC serial data transmission flow chart

Step 7: The register C located in data transmission module of FPGA/CPLD will transmit data in accordance with data transmission or storage module serial interface clock domain requirements in sequence, when the data come. Otherwise, C will wait for the data's coming, and when the register B becomes 1, register C in one clock period of data transmission module in FPGA/CPLD will receive the data of register A located in receiving module of FPGA/CPLD, and then the value of register D will be set to 1;

Step 8: The register C sends data to serial transmission or storage module in the clock domain of transmission module in FPGA/CPLD. Serial interface sends parallel data as serial way out once 1bit or sends to next unit for further serial interface processing;

Step 9: If the value of register D becomes 1 in receiving module of FPGA/CPLD, set the value of register B to be 0. Then the register A in receiving module data of FPGA/CPLD follows step 5 required to receive data;

Step 10: when the register C in transmission module of FPGA/CPLD follows data transmission demand or serial requirement of the storage module serial to finish the transmitting of the data, set the value of register D to 0;

Step 11: Judge whether the acquisition process is over or not. If it is not over, return process to step 6, or end the entire program.

C. CDC Serial Data Transmission Realization

In the realization of one certain type of near-surface FEM instrument, we choose AK5394A ADC of AKM. This Delta-Sigma ADC is dual channel 24-bit ADC, with 192 kHz sampling rate. We adopt programmable logic digital device LCMXO2-1200Z-1TG100 of Lattice and digital signal processor DSP56311 of Freescale. And the synchronous serial port is employed to receive data.

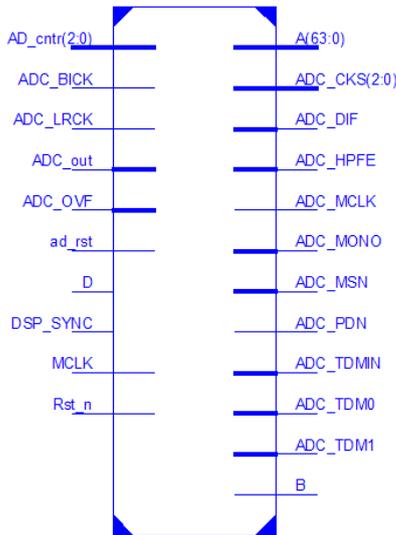


Fig. 7. AK5394 interface and serial-to-parallel conversion

As shown in Fig. 7, the Delta-Sigma ADC interface part for the realization of the method proposed, owns AK5394 inherent timing control interface and serial output interface ADC_out, in addition to the A interface and registers B and D. The bit width of A is 64bit, which is composed of 2 channel data, channel flag and start stop

As shown in Fig. 8, C is the data register interface, and B and D are corresponding to flag registers respectively. DSP_XDATA is the serial interface. And other signal interfaces are for control signals of digital signal processor DSP56311 and reset lamp signal of the module itself.

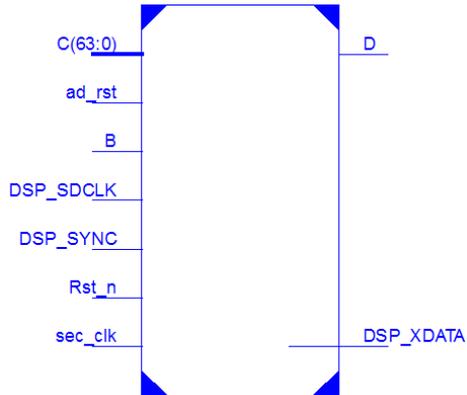


Fig. 8. Transmission interface and parallel-to-serial conversion

In Fig. 7 and Fig. 8, A and C are connected together as the connection channel of this two modules. As interconnection control signals of these two modules, registers B and D guarantee correct data transmission.

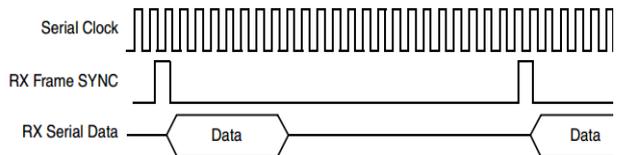


Fig. 9. The realized DSP56311 receiving serial interface timing sequence [7]

The control timing of processor DSP56311 is shown as Fig. 9. In the whole design, the serial data interface rates of AK5394A and DSP56311 are not the same. The former output rate is 6.144MHz, while the latter one is 20 MHz [7], [8]. Serial data acquisition and transmission under different clock domain is adopted for these two modules.

IV. TEST RESULTS AND PERFORMANCE COMPARISON

A. Data Output Test

In actual test, the data through the digital signal processor DSP56311 chip go through the Ethernet of ARM chip AM3354 produced by TI and is shown on the terminal display of PC. And judge whether the data are smooth and missing or not through observing the data.

As you can see from Fig. 10(a-d), the ordinate stands for amplitude, and the abscissa means sampling points. Noise curves stand for random noise, and the curves are smooth and with no singularity. The scale of abscissa can show noise randomness to prove the validity and reliability of this method. And this method can be proved to satisfy the CDC serial data transmission in geophysical instruments.

Nine charts with decreasing sampling point are shown in Fig. 11(a-d). From different frequency test charts, we can see that the first 3 pictures are with sine very smooth wave lines. In last chart, there are 5 points between two scales. And for the corresponding 5 data, there is no smooth improvement, so the data of the whole chart can be achieved completely without omission.

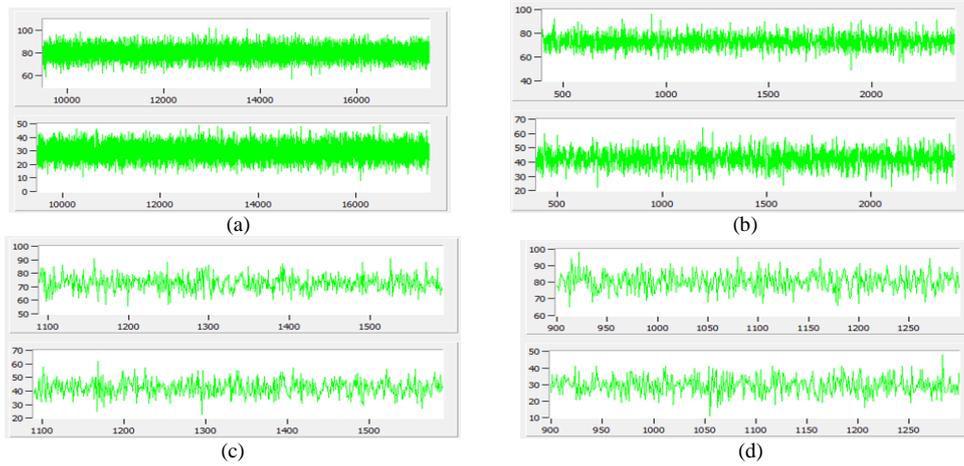


Fig. 10. Geophysical instrument front-end noise measurement

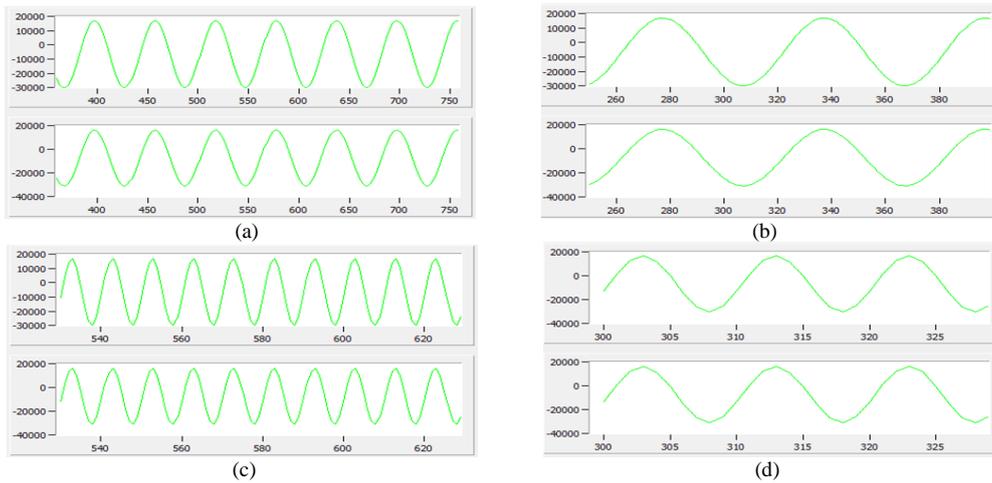


Fig. 11. Sine wave continuous test chart

B. Performance Comparison

The main comparative object of the method proposed is traditional CDC data transmission. The method has advantages in many aspects, which are shown in Table I.

TABLE I: COMPARISON WITH TRADITIONAL METHOD

		New Method	Traditional Method
1	Resource Utilization	Need not FIFO	Need FIFO with certain depth
2	Power Consumption	Small	Slightly large
3	Costs	Small	Slightly large
4	Volume	Not increase	Increase unless without FIFO
5	Rate	It depends	It depends

From Table I, we can see that the method composed can achieve the same function. But as to the comparison with employing FIFO chip, because the traditional method adds FIFO module or FIFO chip, the size is bigger, and power consumption, cost and resource utilization are larger relatively. Therefore, the proposed CDC serial data transmission method is more superior.

V. CONCLUSION

As the core part of geophysical instruments, data acquisition puts emphasis on its every process. And power-consumption reduction, resource optimization and cost reduction lead to the need of omnidirectional considerations in the whole geophysical instrument design process. For the CDC serial data transmission problem encountered, designers commonly adopt FIFO chip or design FIFO function module in digital programmable logic chip FPGA/CPLD to work under different clock for seamless serial data transmission and interaction.

For the existing programmable digital logic device FPGA/CPLD of geophysical instruments, we take use of simple data registers and flags register, when doing the conversion between parallel data and serial data in the CDC interface, to do effective data transmission under different clock working mode for the realization of CDC serial data interaction.

In the near-surface FEM instrument design, we implement CDC serial data transmission module in programmable digital logic chip using the method we have proposed, which combines with Sigma-Delta ADC, low-power programmable digital logic chip CPLD

produced by Lattice and digital signal processor. Do data acquisition test on noise and effective data for geophysical instruments containing CDC serial data transmission module to verify the feasibility and availability of this method

In contrast to the conventional method, the method we proposed not only can implement function as the conventional method, but also can save FIFO resources. And there is a great improvement in power consumption, cost, resource utilization and volume.

The method proposed is not only applied in a near-surface FEM instrument successfully, but also made full use in some audio-frequency magnetotelluric instruments. And we can also apply this method to CDC serial data transmission and exchange in many other data acquisition process, as well as to geophysical instruments.

ACKNOWLEDGMENT

This work was supported by the National Science and Technology Infrastructure Funds of China (Grant No.2013FY110800), National Natural Science Funds of China (Grant No.41174103), National High Technology Research and Development Program of China (863 Program) (Grant No.2014AA06A615), the Fundamental Research Funds for the Central Universities of Central South University(Grant No.2015zzts065), all support is gratefully acknowledged. Thanks Ru-Jun Chen, Hai Dong and Champion Geophysical Technology (Hunan)'s related researchers for their guidance and help. The authors would like to thank the editor and the anonymous reviewers for their valuable comments.

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