A Regulator Design for a SerDes PHY of a High Speed Serial Data Interface

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Abstract —A fully integrated 3.3 V-to-1.2 V supply voltage regulator for application in IEEE 1394B PHY has been designed in 0.13μm SMIC Mixed Signal process technology. The regulator is able to deliver peak current transient of 300 mA, while the output voltage remain within a margin of 10% around the nominal value. The PSRR response larger than 52 dB for frequencies up to 10 kHz under the condition of I_L=300 mA. The FOM of the circuit can be better than 2.5. The circuit can be used in all types of high speed serial data communication system.

Index Terms—On-chip voltage regulator, IEEE 1934B PHY, class-AB.

I. INTRODUCTION

IEEE1394 is an important kind of SerDes interface. A Serializer/Deserializer (SerDes pronounced sir-dees) is a pair of functional blocks commonly used in high speed communications to compensate for limited input/output. These blocks convert data between serial data and parallel interfaces in each direction. Although the term "SerDes" is generic, in speech it is sometimes used as a more pronounceable synonym for SGMII.

IEEE1394 is a standard which is developed by American Institute of Electrical and Electronics Engineers (IEEE) in 1995, the purpose is to provide a low-cost and fast transmission speed serial interface, which have the speeds of 400Mb/s,800Mb/s, 1.6Gb/s and 3.2Gb/s. Now the transmission distance is 4.5m, to be further extended to 50m. The type of this communication has the advantage of high reliability and high data transfer volume over than that of parallel system.

The predecessor of IEEE1394 was called the FireWire, which was completed in 1987.

The majority of industrial FireWire applications involve digital cameras. Such applications could be generically categorized as "machine vision" applications, but this is a very broad term. As FireWire is getting more recognized as a reliable solution for such "machine vision" applications, different types of industrial applications have also emerged. [1]

FireWire hard disks are extensively used in storage solutions and hold a considerable portion of the FireWire market.

It was defined as an IEEE1394-1995 technical specification by IEEE in 1995, before making the serial interface standard, the IEEE 1393 standards have been used, thus the serial number of 1394 this serial number was given, and it is called the IEEE1394, hereinafter referred to as 1394. Because in IEEE1394-1995 and some vague definition, so there comes a supplementary document P1394a, to clarify the doubt, correct and add some functions. In addition, from what has been discussed, the P1394b added new functions in interface standard. As a standard of the working party, P1394b is a high transfer rate and long version of IEEE1394. In this scheme, an important feature is that under the different transmission distance and transmission rate can use different transmission medium.

Network equipment will exchange signals by the digital interface. When connecting multiple devices, such as audio, video, control interface and so on, it is important to consider the all kinds of signals that pass these devices in the way of information transmission, transmission speed, transmission capacity, and cable length. [2]

FireWire applications include:

- Robotic Control. Such systems use FireWire cameras as "environmental sensors". The computer "sees" the environment through FireWire cameras, performs image analysis and provides movement instructions to robotic "hands" that need to interact with the environment (pick up objects, place objects into new positions, etc).
- Automated Optical Inspection. Such systems use FireWire cameras to take "photos" of products manufactured in automated assembly lines (e.g. PC motherboards, PC adapters, cell phones, etc) and examine whether the said artifacts appear as if they have been constructed properly (i.e. they have no visible discrepancies).
- Medical Imaging. Such systems might use FireWire cameras to create 3-dimensional models of a patient's face or body. These models are then used in various ways through the medical procedures.

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- Filming. Such systems might use arrays of FireWire cameras to create special 3-dimensional visual recordings used in special visual effects.
- Security Surveillance. FireWire cameras are used to monitor places of interest for security reasons.
- Storage High performance external hard disks for storage and backup.
- Communication Systems. FireWire is used as an internal local network in data centers for high speed server-to-server communications.
- Audio & Pro-Audio. Specialized audio applications like amplifier/speaker control, audio channel routing/mixing, audio stream delivery for theater systems and concerts, etc, are done with FireWire.
- Set-Top Box. By FCC regulation all set-top boxes in the USA are required to have a functional FireWire port to permit recording of digital content.
- Digital Camcorders. Many digital camcorders provide a FireWire port to allow easy connectivity to the user's personal computer.
- Commercial Aviation. Such systems use FireWire as a high-capacity local network that can also provide the "Quality of Service" (QoS) required for on demand video streaming in in-flight entertainment systems.
- Military. FireWire is being used as a reliable, high-capacity local network that carries control information and sensor data all over a military aircraft, helicopter or vehicle.
- Automotive. FireWire is making strong efforts to get established as the "in car" communications network for modern and future cars, where services like on demand video, TV, music will be available per passenger seat.

In summary, IEEE1394 being as an industry standard high-speed serial bus, has been widely used in digital cameras, TV set-top boxes, home consoles, computers and peripherals. A new generation products, such as DVD, hard disk video recorder, etc. will also use IEEE1394. Its widely application in the digital video and audio consumer market opens up a whole digital photography to manufacture environment for the domestic market and even professional market. IEEE1394 interface has being used in some camcorders in some factory, such as a series of DVCAM recording equipments launched by Sony, DVCPRO25 series devices launched by Panasonic. Other manufacturers are responding with their own camera products, the application of 1394 will be reached to the new height.

The basic SerDes function is made up of two functional blocks: the Parallel In Serial Out (PISO) block (aka Parallel-to-Serial converter) and the Serial In Parallel Out (SIPO) block (aka Serial-to-Parallel converter). There are 4 different SerDes architectures: (1) Parallel clock SerDes, (2) Embedded clock SerDes, (3) 8b/10b SerDes, (4) Bit interleaved SerDes.

The PISO (Parallel Input, Serial Output) block typically has a parallel clock input, a set of data input lines, and input data latches. It may use an external Phase-locked loop to multiply the incoming parallel clock up to the serial frequency. The simplest form of the PISO has a single shift register that receives the parallel data once per parallel clock, and shifts it out at the higher serial clock rate. Implementations may also have a double-buffered register. The SIPO (Serial Input, Parallel Output) block typically has a receive clock output, a set of data output lines, and output data latches. The receive clock may have been recovered from the data by the serial clock recovery technique. However, SerDes which do not transmit a clock use reference clock to lock the PLL to the correct Tx frequency, avoiding low harmonic frequencies present in the data stream. The SIPO block then divides the incoming clock down to the parallel rate. Implementations typically have two registers connected as a double buffer. One register is used to clock in the serial stream, and the other is used to hold the data for the slower, parallel side.

Some types of SerDes include encoding/decoding blocks. The purpose of this encoding/decoding is typically to place at least statistical bounds on the rate of signal transitions to allow for easier clock recovery in the receiver, to provide framing, and to provide DC balance.

The transmission of 1394 interface is implemented by the protocol layer, and it can be divided into physical layer, link layer and process layer.

Processing layer: used to implement the request and response signal.

Link layer: provide transmission services for packets that have the asynchronous and synchronous transmission function. Provide the electrical and mechanical connection between 1394 cable and 1394 devices. In addition to the completion of the actual data transmission and reception tasks, it also provides initial setup (Initialization) and Arbitration (Arbitration) service, to ensure that only a node transmits data at a moment and make all of the devices on the bus can accessed as well.

IEEE 1394B PHY provides the analog transceiver functions needed to implement a one-port or two-port node in a cable-based IEEE 1934B network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, and for packet reception and transmission. This PHY is powered by a single 3.3-V supply. An internal (1.8V/1.2V) voltage regulator supplies the core voltage supply. To protect the analog circuitry from noise, all analog power VDD and GND are separated and decoupled with capacitors.

Fig. 1 shows the circuitry needed to allow 3.3V operation in IEEE 1394B PHY. The external 3.3 V (VDDD) is connected to the integrated supply voltage regulator and the I/O cells. The function core operates at 1.2 V generated by the regulator.

The I/O cells convert the 1.2 V logic swing to 5 V swing and vice versa. For being compatible with exiting

3.3 V IC's, there is not always an IC pin available for external decoupling of the internal 1.2 V supply. Therefore, the regulator itself must be able to deliver a stable and accurate internal supply voltage, without using an external capacitor. This is difficult to realize since the internal function core, including digital circuits, draws large and steep supply current peaks. Both the external 3.3 V and internal 1.2 V supply voltages have the normal ±10% tolerance.

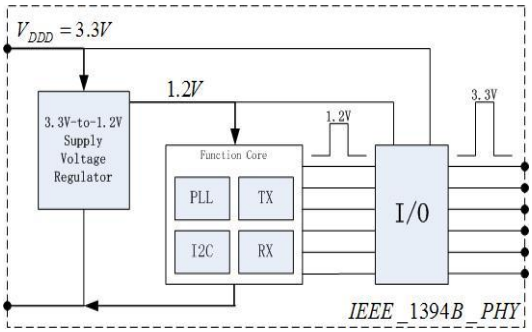

Fig. 1. Application of the regulator in IEEE 1934B PHY.

Since the supply voltage regulator needs to be fully integrated, no high-efficient dc-dc converters which need external inductors and/or capacitors can be used. This regulator must therefore be of the series regulator type, so it will be dissipating power. This does not have to be a problem since a 3.3 V technology IC would also have had a larger power dissipation due to the larger internal voltage swings and parasitic capacitors. The total power dissipation of a 1.2 V function core plus supply voltage regulator is less than the same function in a 3.3 V technology. The external supply voltage is the same while the current is reduced [3], [4].

Since the PHY is powered by a single 3.3 V supply, the integrated regulator can be designed in such a way that the external supply voltage can be anywhere in the range of 3.0-3.6 V.

Summarizing, the regulator to be designed must be fully integrated, being able to deliver steep current transients and having an absolute accuracy of ±10%. Also, the external VDDD must be anywhere in the 3.0-3.6 V range, and the circuit must be small and have a small standby current. In addition, the circuit must have a power-down mode in which the current consumption is reduced to several microamperes.

II. Circuit Design and Implementation

The fully SerDes transceiver is shown in Fig. 2. It mainly consists of receiver (RX), transmitter (TX), CDR, common part and PLL. Some digital parts like 8B/10B encoder/decoder, I2C, built-in self test (BIST) have also been implemented on-chip but they are beyond the scope of discussion in this paper. The final baud rates become 125Mb/s, 500Mb/s and 1Gb/s with 8B/10B coding/decoding in the SerDes transceiver to meet the standard data rates of 100Mb/s, 400Mb/s, and 800Mb/s as defined by the standard.

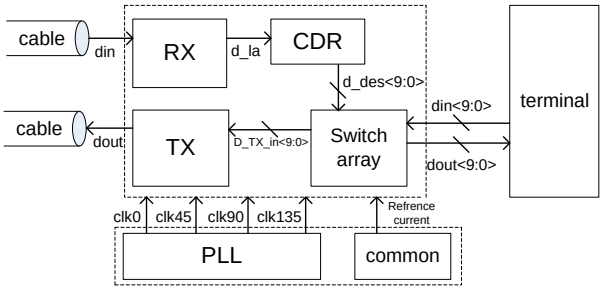

Fig. 2. Top view of transceiver

The structure of RX is shown in Fig. 3. The RX contains preamplifier, equalizer, limiting amplifier and signal detector. An equalizer is used following preamplifier to compensate for the channel loss. In conventional design, four general kinds of receiver equalizers for over Giga data transmissions are presented: passive-component equalizer, active continuous-time equalizer using split-path amplifier, active equalizer using discrete-time finite impulse response (FIR) filter and active equalizer using continuous-time FIR filter. In this work, an active continuous-time equalizer using split-path amplifier is applied for cost and performance consideration. This kind of equalizer works without knowing the information of data and clock. The equalized signals are reshaped by the following limiting amplifier, which is then sent to CDR for further processing. On the other hand, a signal detector circuit is applied for tone test process as specification required.

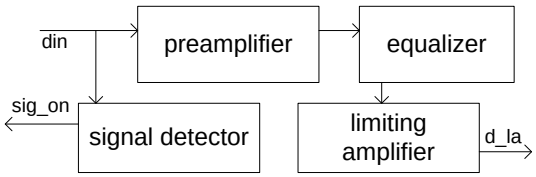

Fig. 3. Receiver

The CDR is a critical part of the SerDes system. In this design, a PI based CDR is designed which is shown in Fig. 4. The proposed CDR composed of slicer, deserializer (it contains 1-to-2 deserializer and 2-to-10 deserializer), PI, digital filter and a frequency divider is plotted in Fig. 5.The clock divider provides full data rate clock for different operation mode while the PI always provides 1GHz clock. In order to obtain better linearity, averaging process and digital control are applied.

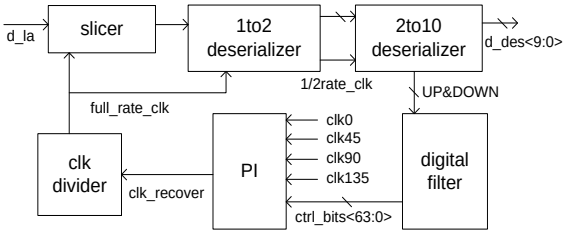

Fig. 4. Clock and data recovery

The TX which is shown in Fig. 5 dominates the function of receiving the parallel data from the logic core, transferring the parallel data into serial data before

sending it out to cable. It consists of serializer and line driver with pre-emphasis.

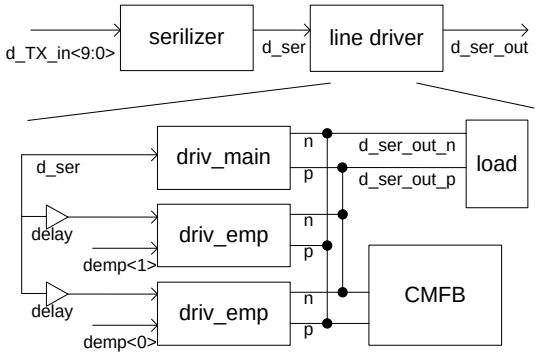

Fig. 5. Transmitter

The serializer outputs the full rate data to the line driver, and the line driver accomplishes the function of pre-emphasis. The pre-emphasis at TX is an important part to overcome the poor high frequency characteristics of the channel. In this work, we adopt a low cost symbol-spaced FIR filtering based pre-emphasis cell in line driver for its simplicity.

A fully integrated PLL is designed to provide the clock network for the whole system without any external component, and is compatible with the different operation mode defined by the IEEE1394b protocol to coordinate the operation of all the blocks, ports and nodes. As been shown in Fig. 6, the PLL consists of phase/frequency detector (PFD), differential charge pump, second order low pass loop filter, quadrate phase VCO and feedback frequency divider. In order to improve duty cycle of output clock to accommodate possible double edge operation in digital parts, duty correction technique is employed in the divider.

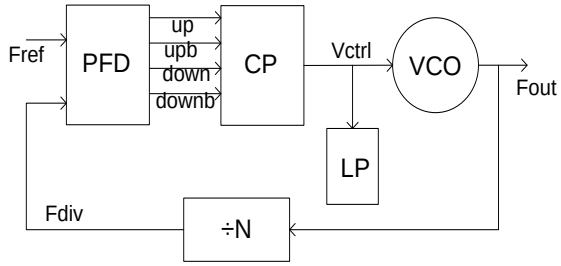

Fig. 6. Phase locked loop

The regulator is a block of the common. Fig. 7 shows the architecture of the proposed LDO regulator, which consists of a NMOS pass transistor in a source-follower configuration, a class-AB push-pull error amplifier and a bandgap 1.2 V voltage reference.

Bias generation provides precise band-gap voltage reference, a bank of bias signal for SerDes of each port and cable power monitoring. Bandgap consists of a built-in band-gap core, and bias bank for both shared analog circuit and SerDes of each port. Bandgap core produces a precise voltage reference with low temperature coefficient (below 100ppm) and low PSRR. Two types of current are generated for various sub-blocks.

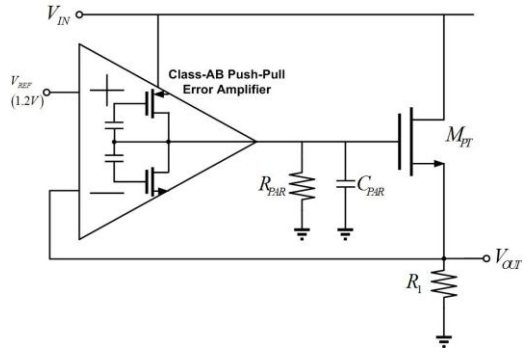

Fig. 7. Architecture of the proposed regulator.

A. Pass Transistor

As the drop-out voltage between V_{IN} and V_{OUT} is around 2.1 V, a NMOS pass transistor is chosen. Furthermore, it has a number of performance advantages over PMOS pass transistor, regardless of its efficiency draw back.

Stability: NMOS pass transistor connected in a common-drain (source follower) configuration is a good buffer when driving capacitive loads. The output impedance of a NMOS pass transistor is approximately $1/(g_{m,N}+g_{mb,N})$ instead of $r_{o,p}$ for a PMOS pass transistor, pushing the output pole of the regulator to very high frequency. Thus, the linear regulator would always be stable as long as the rest of the circuit (error amplifier) is properly compensated.

Area: A regulator using NMOS pass transistors require less die area, because a NMOS based pass transistor would be smaller than a PMOS one due to better mobility of majority carriers (electrons vs. holes): μ_n can be three times as large as μ_p. Thus, to achieve the same $R_{ds,on,}$ NMOS would need smaller W/L ratio, which translates to smaller area WL given the same channel length L is used. This can be a major consideration for area efficient applications, because pass transistors usually occupy most of the die area within a regulator.

Power Supply Rejection: A NMOS regulator would generally have better PSR because an NMOS common-drain output acts like a cascade device for the output node. PMOS common-source configuration, however, does little to shield the supply ripple, since the supply is directly connected to the source.

Load Transient: A NMOS regulator has smaller source resistance $1/(g_{m,N}+g_{mb,N})$ before and after close-loop feedback. Therefore, a NMOS regulator would experience less voltage undershot and overshot during abrupt load current changes.

B. Error Amplifier

In order to improve the transient response of the regulator, the conventional error amplifier is replaced with a class-AB push-pull amplifier. [5]

Fig.8 shows the schematic of the proposed error amplifier. It consists of a folded-cascode stage M1-M10 and an output stage M17-M18 with floating class-AB control transistors M11-M12.

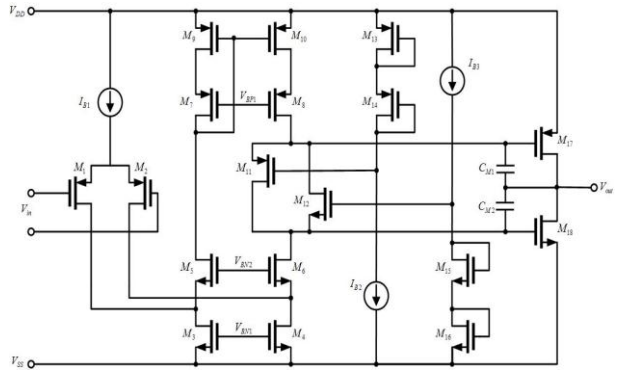

Fig. 8. Schematic of the proposed class-AB push-pull error .amplifier

The output stage transistors M17-M18 are common-source connected, which are directly driven by the output current of the folded-cascode stage. The stacked diode-connected transistors M13-M14 and M15-M16 bias the gates of the class-AB transistors M11 and M12, respectively.

The floating class-AB control transistors, the stacked diode-connected transistors and the output transistors set up two translinear loops M11, M13, M14, M17 and M12, M15, M16, M18, which determine the quiescent current in the output transistors. The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. Suppose the in-phase signal current sources are pushed into the class-AB output stage. As a result, the current of the P-channel class-AB transistor increases while the current in the N-channel class-AB transistors decreases by the output transistors move up. Thus the output stage pulls a current from the output node. This action continues until the current through the P-channel class-AB transistor is equal is kept at a minimum value, which ban be set by W over L ratios of the class-AB control transistors. A similar discussion can be held when input signals are pulled from the class-AB output stage.

C. Frequency Compensation

The regulator is compensated using the conventional Miller technique. The capacitor C_{M1} and C_{M2} around the output transistors, M17 and M18, split apart the poles. There are three poles located at the output of the folded-cascode amplifier (ω_d), the gate of the pass transistor (ω_L) and the output of the regulator (ω_{out}) respectively.

$$\omega_d = \frac{g_{m1,2}}{C_{M1,2}}$$

$$\omega_{out} = \frac{g_{m,out}}{C_{PAR}}$$

$$\omega_L = \frac{g_{m,PT}}{C_L}$$

where $g_{m1,2}$ is the transconductance of the input differential pair of the error amplifier, $g_{m,out}$ is the transconductance of the output transistors of the error amplifier, $g_{m,PT}$ is the transconductance of the pass transistors, $C_{M1,2}$ is the parasitic capacitor of the input differential pair, C_{PAR} is the parasitic capacitor at the gate of the pass transistor and C_L is the load capacitor. The ω_d, the dominant pole, is in the low frequency range, and the other two poles are both pushed to very high frequency ensuring a 20 dB per decade roll off of the amplitude characteristic [6].

III. Simulation Measurement Results

The layout of the regulator is shown in Fig. 9.

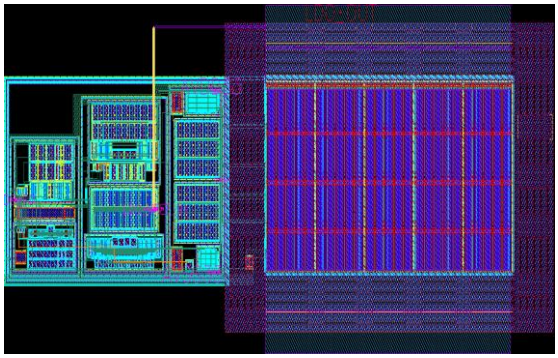

Fig. 9. Layout view of the regulator.

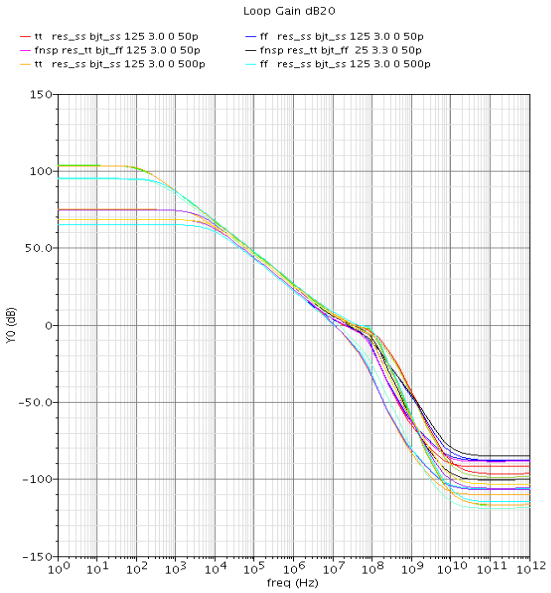

Fig. 10. Simulation results of the loop stability-gain.

The voltage regulator is simulated for loop stability on various corners, shown in Fig. 10 and Fig. 11. The load capacitor is 50 pF, and the least phase margin is around 45° .

The parameter of PSRR is the most important of a regulator. It shows the variation of power supply affecting the output voltage of the regulator. It is defined as:

$$PSRR = A_v(V_{dd}=0) / A_{dd}(V_{in}=0)$$

where Av is the differential gain of the amplifier when the V_{dd} has no variation. And the Add is the differential gain when the V_{in} has no input.

Fig. 12 shows the power supply rejection ratio (PSRR) for I_L=300 mA on various corners. Simulation results

reveal a PSRR response larger than 52 dB for frequencies up to 10 kHz. For I_L=300 mA on various corners. Simulation results reveal a PSRR response larger than 52 dB for frequencies up to 10 kHz.

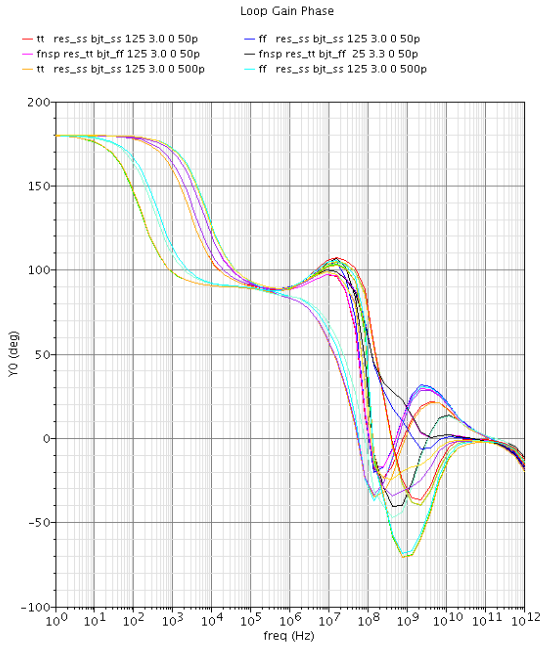

Fig. 11. Simulation results of the loop stability-phase.

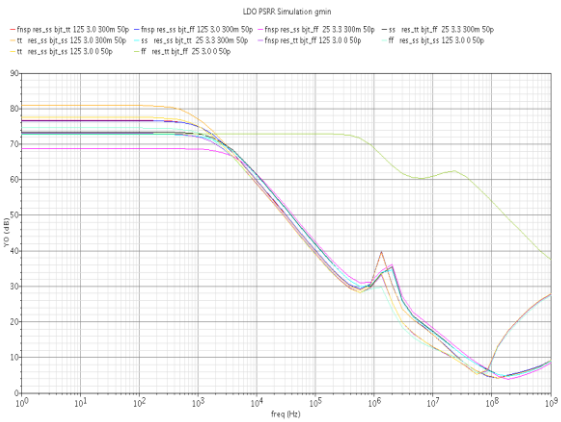

Fig. 12. Simulation results of PSRR.

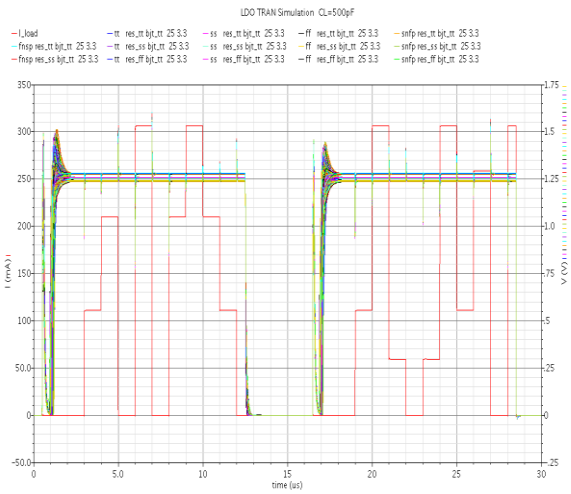

Fig. 13. Simulation results of transient performance.

The regulator is then subjected to a 0-300 mA load transient current with 10 ns rise and fall times on various corners, as shown in Fig. 13. An extra ringing, less than 120 mV, is experienced for the positive load current transition, but the ringing quickly subsided and a stable response is reached within 2us in the worst case.

In order to provide a clear picture of the performance in the proposed regulator resulting from the Class-AB push-pull error amplifier, a comparison of some reported regulators is given in Table I. A figure of merit FOM=I_L/V_{ripple} is adopted to compare the load transient response of different regulators by evaluating the tradeoffs between the load current IL and the load transient ripple voltage V_{ripple}.

The larger the FOM, the better the load transient response the regulator achieves. From Table I, the proposed regulator achieves the largest FOM compared with other reported regulators.

TABLE I: PERFORMANCE COMPARISON WITH PREVIOUS REPORTED REGULATORS

	1998 [3]	2009 [7]	This work
Technology (μm)	0.35	0.35	0.13
Supply Voltage (V)	5.0	1.8	3.3
Output Voltage (V)	3.3	1.0	1.2
Dropout Voltage (V)	1.7	0.8	2.1
Load Current I_L (mA)	300	100	300
Quiescent Current (mA)	0.75	0.1	1
Load Transient Ripple V_{ripple} (mV)	-	450	120
ESR Required	No	No	No
FOM (S)	-	0.22	2.5

The layout of all the SerDes circuit is shown in Fig. 14, for this work is only a small part of it, it is not be shown separately, the regulator is in the part of "common". The chip has been fabricated by using 0.13μm technology.

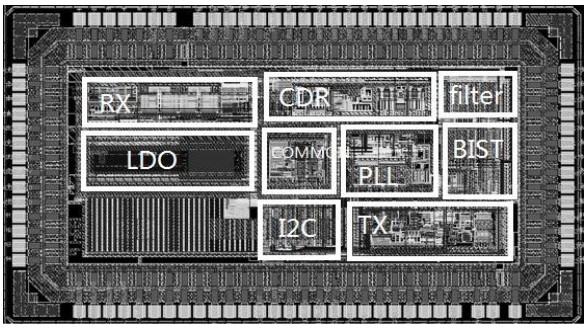

Fig. 14. Layout of the all SerDes transceiver

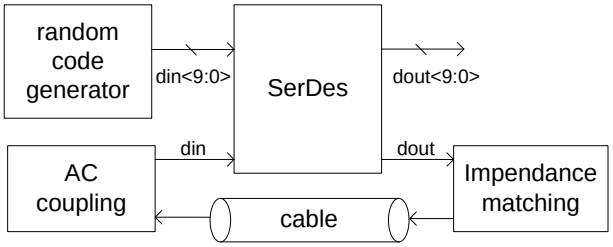

Fig. 15. Testbench of the all SerDes transceiver

The testbench is illustrated in Fig. 15. A loopback test simulation is carried out, which loops the transmitted data back into the receiver. To simulate the channel characteristics of long transmission distance, RLC transmission-line model for 100-m UTP (unshielded twisted paired) is adopted. The RLC model for 100-m UTP described in [8] is shown in Fig. 16. For short transmission distance, we directly connect the impedance matching circuit to the ac coupling circuit.

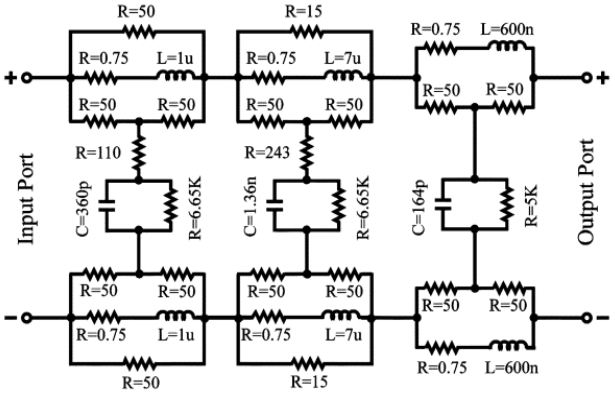

Fig.16. RLC transmission-line model for 100-m UTP

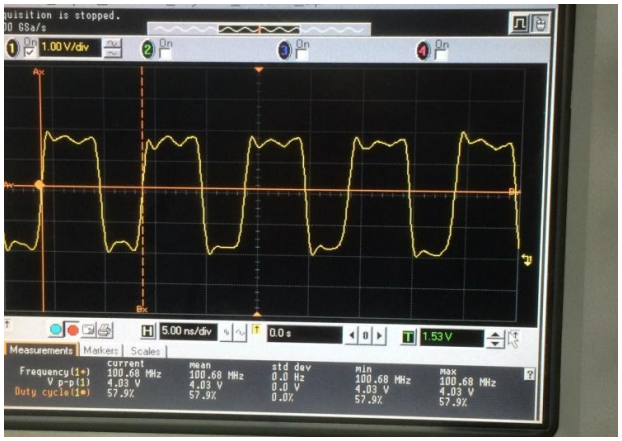

Fig. 17. Measurement result of CDR (S800)

Fig. 18. Measurement result of CDR (S400)

The measurement results of CDR are shown in Fig. 17 to Fig. 19. The frequency is presented in the Table II. The jitter measurement: P_P=649ps, rms=108ps.

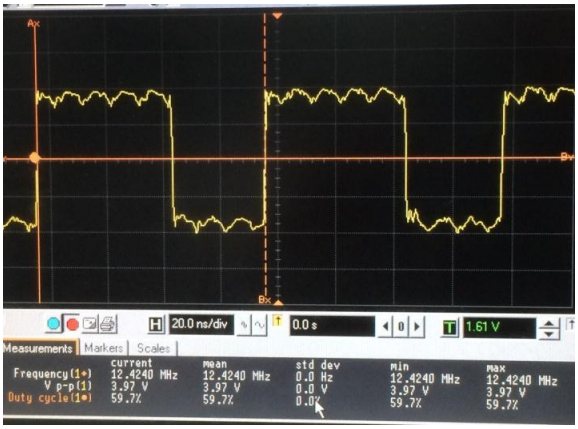

Fig. 19. Measurement Result of CDR(S100)

TABLE II: FREQUENCY OF CDR OUTPUT

Mode	Frequency	Vpp
S800	100.68MHz	3.96V
S400	49.9MHz	3.88V
S100	12.4MHz	3.97V

At S800, conduct one-stage eq_stage, the DC gain of the rx_preamp is -3dB, the frequency compensation is 400MHz，peaking gain is 4.4dB, the DC gain of rx_eq is 0dB, the RX differential input signal frequency is 250MHz,the measurement results of the ten parallel outputs is shown in Fig. 20.

Fig. 20. Measurement of RX parallel outputs at S800

When 20% pre-emphasis is enabled in TX, after equalization, the eye is restored with jitter less than 154ps, the measurement results of the output eye diagrams are shown in Fig. 21.

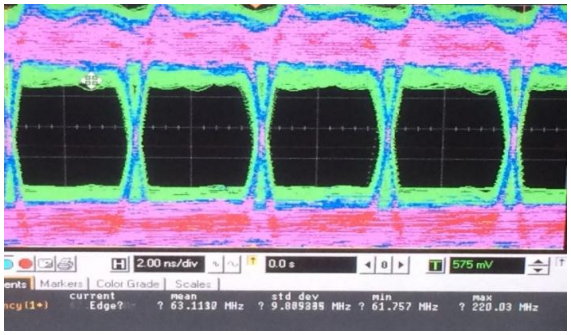

Fig. 21. Eye diagrams of the TX

The measurement result shows that the regulator provides a good function for stabilize the core supply voltage. And make the all SerDes worked reliably.

IV. Conclusions

SerDes is now pervasive in communications networks and used extensively in applications such as laptop computers, office imaging, industrial vision, test and measurement, medical, and automotive. It provides an attractive solution - a small-swing differential signal for fast data transfers at significantly reduced power and with excellent noise immunity. Along with the applications, SerDes continued to evolve over the last decade to meet specific requirements such as high speed data communication. For example, the latest SerDes products are capable of data rates in excess of 5 Gbps while still maintaining the low power and noise immunity characteristics.

This paper focus on the design of an embedded 3.3V to 1.2V supply regulator for IEEE 1394B PHY. It has been fabricated in a 0.13μm SMIC Mixed Signal process technology. The circuit is able to deliver the steep supply-current transients for function circuits while the output voltage remains within ±10% accuracy. The PSRR response larger than 52 dB for frequencies up to 10 kHz under the condition of IL=300 mA. The FOM of the circuit can be better than 2.5. The circuit needs no large (external) capacitor across the internal 1.2 V.

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