Design Concepts and First Implementations for 24 GHz Wireless Sensor Nodes

Stefan von der Mark, Meik Huber and Georg Boeck
Technische Universität Berlin, Microwave Engineering, Berlin, Germany
Email: boeck@tu-berlin.de

Abstract— **This paper reviews proposed realization concepts and achievements of wireless sensor nodes and focuses on new developments in the 24 GHz frequency range. The relatively high frequency offers the advantage of ultra miniaturization and therefore opens new application fields. On the other hand power consumption of the RF-front-end becomes still more challenging than at lower frequencies. It is shown that by applying very simple CMOS transceiver architectures and modulation schemes combined with innovative efficient wake-up concepts, very low energy consumption can be achieved. Technological realization concepts and first experimental results from a 24 GHz demonstrator as well as novel special purpose wakeup-circuitry are presented, too.**

Index Terms—**Wireless Sensor Networks, low power, wakeup, CMOS, K-band**

I. INTRODUCTION

Similar to the evolution of wireless communication systems, variety, functionality and performance of wireless sensor networks are rapidly increasing. The sensors transform physical, chemical and biological parameters into information. These parameters and the related signals can be very different and vary from characterizing home, office or traffic environment up to characterization of animals and humans.

The sensor network is formed by a cluster of locally distributed sensor nodes connected with each other by wireless communication paths. Because of energy saving reasons, communication channels between all nodes cannot permanently exist. Two methods can be applied for establishing connectivity: periodic or individual wake up. The individual wake up offers the advantage that no clock is necessary, which saves battery power but requires more expense on the detection and identification side. Therefore, synchronization between the active nodes and autoconfiguration are necessary and very challenging tasks. Further, each "member of an active cloud" has to check out the local neighbourhood and to organize its operation in a manner that ensures a maximum longevity of the cloud, while simultaneously assuring the required functionality and performance.

Sensor networks are currently discussed for a wide range of applications ranging from monitoring of rotating machines, factory and warehouse logistics to environmental monitoring, e.g. [1]-[7]. In general, distances between the nodes and data rates of sensor networks are in the order of meters and up to the order of 10 kBit/s, respectively. Especially within the "PicoRadio" and the "WiseNET" projects [5]-[7] fundamental work has been performed and first hardware demonstrators have been realized proving the functionality of the whole network concept. The frequency range used was up to 2.4 GHz.

The miniaturization limit is primarily given by the integration technology and the antennas. On the other hand, aggressive miniaturization of the individual nodes would open new application fields. In this case, the implantation into objects of our daily life like keys, watches, wallets, rings, glasses, bottles caps, books, etc. as well as into creatures becomes more and more imaginable. The way towards these ultra low sized sensor nodes leads to higher carrier frequencies, as antenna size becomes the limiting factor for miniaturization. A first concept for a 24 GHz system was established within the AVM project [8], [9], which concentrates on miniaturization of the nodes.

This paper discusses the AVM system concept with focus on wake-up scheme, RF-architecture, transmission and integration technology. First experimental results from wake-up circuitry and from a 24 GHz demonstrator are presented.

II. WAKE-UP RECEIVER

A. Concept

Besides low power consumption of the whole system during the active state, ultra low power consumption during the sleeping period is important in at least the same manner. Because a duty cycle of less than 10^{-4} between active and sleeping mode is assumed for the nodes, the minimization of the standby current is an ultimate goal and a value in the order of 1 nA is desirable. At the same time an efficient wake-up concept with an energy saving hardware realization is needed.

Nosovic and Todd have proven in [10] that periodic wake-up realizations waste energy because of the serious disadvantage that most of the wake-ups will usually be dispensable. Additionally, because the wake-ups have to be synchronized, permanent energy consumption of the node's clock cannot be avoided and additional energy is needed for the synchronization of the clocks.

Therefore, an individual wake-up concept has been developed during the AVM project [8], [9], the functional principle is given in Fig. 1.

A MOS (or Schottky-diode) detector is "listening" for wake-up signals from neighboring nodes. A wake-up signal consists of a burst (Fig. 1, right) which generates a comparator output signal and activates the subsequent identification chain consisting of LNA, detector and address decoder by dynamic biasing. This much more sensitive identification chain is responsible for detection and recognition of the received address. By this way, the address of the calling node can be transmitted, too. Only in the case of matching between requested and deposited address of the node the most power hungry main transceiver is woken up. In this case the activated node responds to the calling node confirming the successful wake up. Otherwise, the procedure is repeated.

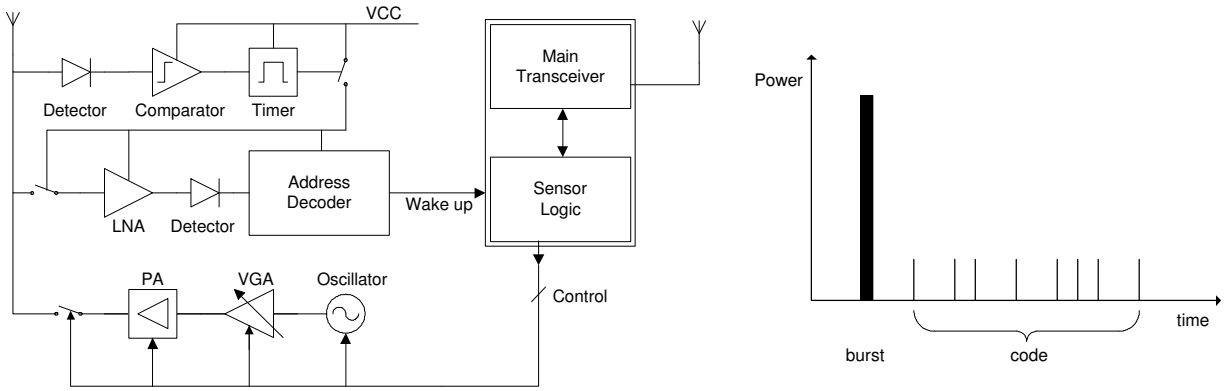

Figure 1. Block diagram of the wake-up circuit (left) and wake-up signal (right).

B. Implementation

To prove the feasibility of this concept, the most critical building blocks have been implemented. The detector which is a central element of the system shown in Fig. 1 was implemented as drafted in Fig. 2 (left). The basic idea is to use cascaded rectifiers to build up a voltage at the gates of a CMOS inverter chain. A bias voltage is added to the detector voltage to bring the inverter very close to the switching threshold. As this voltage is applied to the gates of the MOSFETs through the diode-chain, only the gate leakage current which is far below 1 pA is drawn from the bias source, there is no bias current for the diodes. Schottky diodes with high saturation current I_s are necessary for this purpose to charge the capacitors in the chain at very low RF voltage levels.

Simulations have shown that of all diode parameters, a high I_s is of utmost importance, next important is a low junction capacitance C_j . The series resistance R_s is not much of an issue, as the currents are very low anyway, but lower is better. This has to be taken into account when choosing the diodes for the detector.

Width and length of integrated diodes usually can be scaled. I_s and R_s improve with larger width (increase and decrease, respectively), but unfortunately C_j and other parasitics as well as the reverse current also increase for larger width, degrading the performance. An optimum has to be found for each specific technology.

The closer the bias voltage is to the threshold of the inverter, the more sensitive is the circuit. However, the cross-current through the inverter increases. Again, a trade-off between sensitivity and power consumption has to be found. As lower sensitivity means in turn increased power consumption on the transmitter side, the optimum operating point depends on the intended operation scenario: for sensors that are needed rarely, low standby-power is most important and lower sensitivity can be accepted. The more often wake-up calls happen, the more power is used on transmission of these calls, and thus higher standby power in the receiver can be tolerated for the sake of reduced power consumption for transmission.

C. Results

In [11] we have presented the results for an integrated cascaded detector as described above. Measurements with 1 MΩ load have yielded 0.2 mV DC output at -40 dBm RF input power at 2.4 GHz. The input impedance of the inverter stages is several orders of magnitude higher than that, simulations show that with 10 GΩ load to the detector, which is a very pessimistic assumption of the gate leakage currents, 3 mV can be obtained from mere -50 dBm RF power. According to simulations, this will be sufficient to toggle the inverter stages enabling recep-

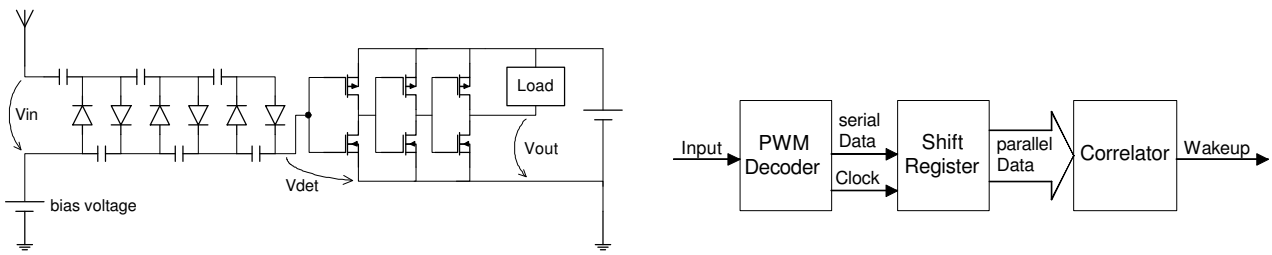

Figure 2. Schematic of the detector (left) and block diagram of the address detector (right).

tion of the data. The complete circuit, including detector and inverter stages, has been integrated for proof of the simulations, it is in production right now and measurements will be published as soon as possible.

Implementation of the following critical stage, the address decoder, has been accomplished using standard off the shelf CMOS circuitry. The block diagram is shown in Fig. 2 (right). As we have shown in [12], a standby power as low as 10 nW is possible with standard components, this current will only be consumed in the short time span after a burst has been received and reception of a possible address is examined (see Fig. 1). By custom design of this circuitry, current consumption most likely can be further reduced.

During reception of a PWM encoded data signal, the circuit consumes about 40 µW and at 50 kB/s, or 75 µW at 100 kB/s, resulting in 20 nWs power consumption for reception of an 8 bit wakeup address.

III. 24 GHz Communication

A. Concept

To overcome the most serious issue of battery lifetime, implementation of ultra low power concepts on circuit, transmission and system level is obligatory. As only suitable device technology, aggressively down scaled CMOS-technologies can be accepted. The number of function blocks in the RF-transceiver has to be reduced to the absolute necessary minimum, the oscillator and – maybe – the low noise amplifier. Conventional (and power hungry) transceiver modules like up-/down- converters and frequency dividers have to be avoided at all events.

These considerations lead to a base band transmission based on-off-keying (OOK-Modulation) scheme as shown in Fig. 3. On the transmitter side the oscillator is directly modulated by the data stream which means it is simply turned on and off by the data bits. This modulation scheme has been shown to be advantageous for use in ultra-low-power environments in [13]. It saves considerable DC-power because the oszillator in the transmitter needs only to be turned on for "high" bits, the duty cycle during the active state can be as low as about 10^{-3}.

On the receiver side, primarily the low noise amplifier determines the power consumption. It has to provide an acceptably low noise figure and enough signal level to the rectifier and it seems that it can hardly be circumvented. Two antenna concepts have been investigated so far – slot and patch antennas. Patch antennas were used for our first demonstrator, while slot antennas were examined in [14]. The signal to noise ratio at the detector input can be improved considerably by suitable RF-filtering. An integrated Schottky diode- as well as a pure CMOS- rectifier have been investigated as detector. Both concepts are applicable - the choice is determined by the available technology: SiGe BiCMOS e. g. provides integrated Schottky diodes as well as low power CMOS circuitry. A base band amplifier provides the necessary signal level for discrimination and base band post processing. Due to the low bit rates, this amplifier can be a quite slow low-bandwidth amplifier with – compared to the LNA – negligible power consumption.

The baseband implementation is not described here. However, because of the low to moderate data rates and short distances owing to sensor networks, the influence of multi path propagation and fading effects is not challenging. Nonetheless, data rate and base band implementation have to be optimized aiming on lowest energy consumption per transmitted bit.

B. Implementation

As a first step a demonstrator cube with $1cm^3$ volume was realized including a patch antenna. No additional external elements were used at all. Fig. 4 (left) shows a drawing of the assembly. For this first realization, six separate 1x1 cm^2 multilayer PCBs were used to form a cube. A circularly polarized patch antenna was integrated into one of the PCBs (Fig. 4 right, [15]). The antenna gain is about 8 dB. In later versions all six surfaces of the cube will carry antennas, providing excellent space diversity as well as energy conservation by directed transmission. The antenna was excited by electromagnetic aperture coupling through a slot in the groundplane of the antenna. The RF-Chips were flip-chip mounted and SMD-technology was used for all remaining components which were mounted on the inner surface of the six PCBs. A photograph of the assembly is shown in Fig. 5. Later versions will be based on specially shaped multilayer flex substrates including the antennas. After complete assembling the flex will be folded to form the cube.

The LNA-chip specially developed for this project has a noise figure of 8 dB and a gain of 12 dB with 2.8 mW power consumption [16]. A low power 24 GHz CMOS oscillator is under development but was not available for the first system tests. Instead, a developed GaAs-HBT oscillator [17] was used with 18 mW power consumption, 4.2 dBm output power and an efficiency of about 15%. A simple temperature sensor was used as data source at the transmit side and an LCD display as data sink at the receive side. Two (instead of one, because of the GaAs-chip which needs 3 V supply) 70 mAh button cells with

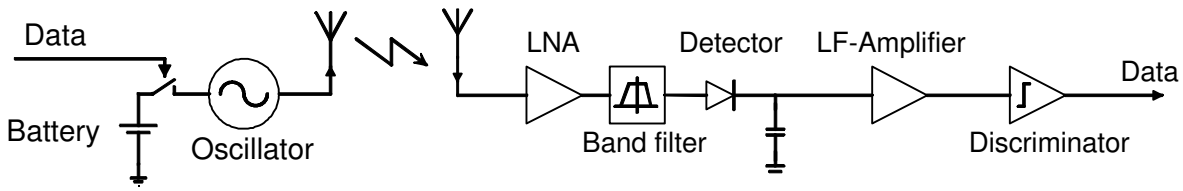

Figure 3. Block diagram of the 24 GHz transceiver

7,3 mm diameter were used as power supply. The cells provide continuous energy for a few hours or – with 10^{-4} duty cycle – for a few years.

C. Results

Reliable data transmission has been demonstrated without the LNA in the receiver, lowering the receiver power consumption to continuous 90 mW [18]. The packet error rate was below 10% for up to 5 cm transmission distance (see Fig. 6). Packet loss was zero up to 8 cm. Data was transmitted uncoded, every packet with at least one faulty bit was considered to be a packet error, while only packets which were not recognized as packet at all were considered to be a packet loss. With error coding as described in [13], the packet error rate could be significantly decreased and data transmission would still

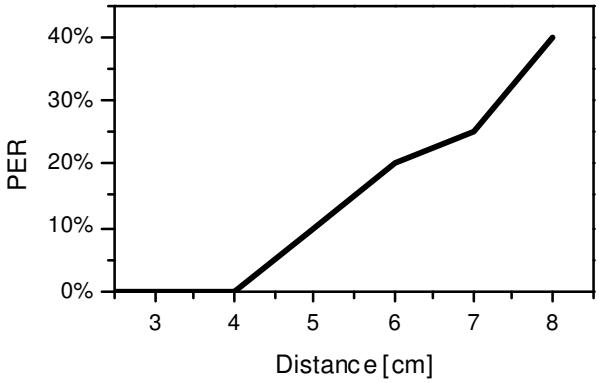

Figure 6. Uncoded packet error rate versus distance.

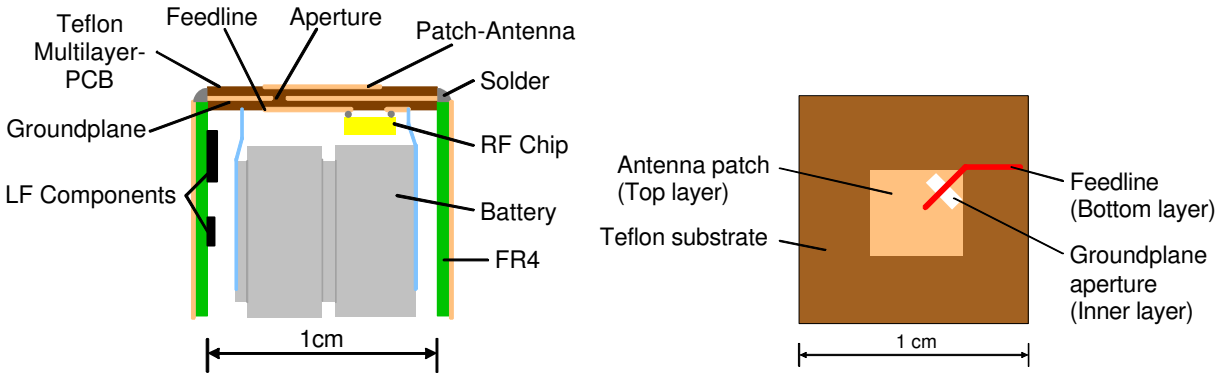

Figure 4. Demonstrator assembly (left) and patch antenna (right).

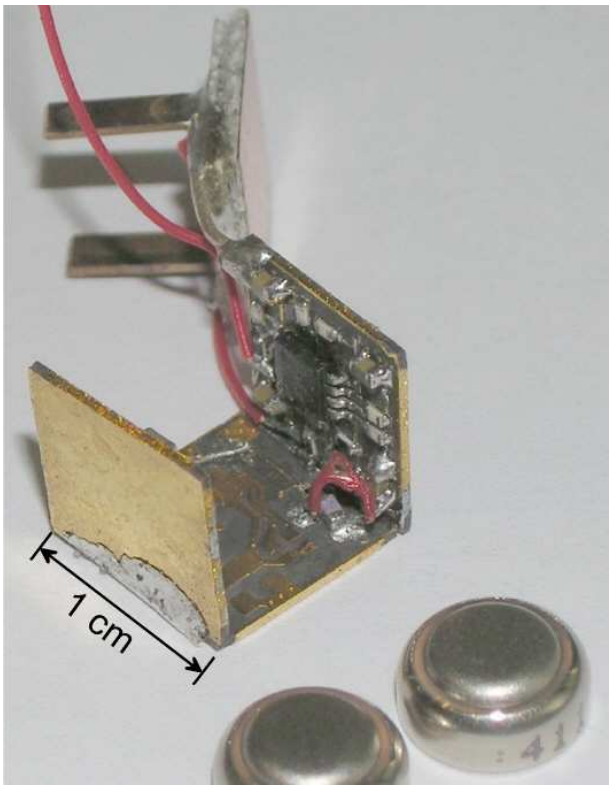

Figure 5. Photograph of the opened cube. The batteries were taken out for better visibility, the antenna patch is on the bottom.

be possible at 8 cm distance and possibly more.

This very short distance communication would be sufficient in some of the visionary smart dust scenarios. To achieve the projected 1 m distance, the LNA will be necessary with then about 20 mW and 5 mW power consumption at the transmit and receive side, respectively. After replacing the GaAs oscillator by the CMOS one we expect a similar power consumption for the transmitter as for the receive part.

IV. Summary and Conclusions

A first implementation of a 24 GHz wireless sensor network was demonstrated. The high operating frequency offers the advantage of serious miniaturization and novel applications. The principal functionality of the data transmission and the wake up system has been shown, a transmission distance of more than one meter can be achieved using a MMIC LNA. In a fully 130 nm CMOS implementation continuous power consumptions in the order of five mW at receive and transmit state can be expected. Assuming a duty cycle of 10-4 this guarantees a network lifetime of at least a few years. From these first results, it can be expected that wireless sensor networks in the millimeter-wave range will emerge to reality during the next years.

Future work will be directed towards fully integrated CMOS sytems-on-chip (SoC), with antenna integration being a crucial part of assembly and packaging technol-

ogy. Localization will also be a key issue and important new feature of the RF part, providing location awareness both for internal network organization (routing, load distribution) and as enabler for location aware services.

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Stefan von der Mark was born in Munich, Germany, in 1975. He received the Dipl.-Ing. Degree in electrical engineering from the Friedrich-Alexander-Universität Erlangen-Nürnberg in 2000.

In 2000 he joined the Fraunhofer Institute for Integrated Circuits in Erlangen, Germany. 2002/03 he was a Visiting Scholar at Rutgers University, NJ, USA, and since 2003 he has been Research Associate and PhD Student at Technische Universität Berlin. His research interests include system and circuit design for sensor networks and ultra low power wireless communications.

Mr. von der Mark is Student Member of the IEEE.

Meik Huber was born in Villingen-Schwenningen, Germany in 1978. He received his M.S. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) in Zurich, Switzerland in 2003.

In 2002/2003 he was a visiting researcher with Prof. Ke Wu at Ecole Polytechnique Montreal, Canada. In 2003, he joined the Microwave Engineering Lab with Prof. Georg Boeck at Technische Universität Berlin, Germany. He developed low power integrated circuits in K-Band and sensor network circuits concepts within the AVM project. Since 2007 he is working as patent engineer with Thomson, Germany.

Mr Huber is a member of the IEEE.

Georg Boeck was born in Wertingen, Germany, in 1951. He received the Dipl.-Ing. degree in electrical engineering and the Ph.D. degree from Technische Universitaet Berlin, Berlin, Germany, in 1977 and 1984, respectively.

In 1984, he joined the Siemens Research Laboratories, Munich, Germany, where his research areas included fiber optics and GaAs electronics. From 1988 to 1991, he was a Full Professor for electronic devices and circuits at the University of Applied Sciences Regensburg, Regensburg, Germany. Since 1991, he has been the head of the Microwave Engineering Lab at Berlin University of Technology, Berlin, Germany. His research interests include characterization, modeling, and design of microwave semiconductor devices, hybrid and monolithic RF- and microwave circuits and systems up and beyond the 100 GHz regime. He has authored or co-authored more than 160 technical papers and one book and holds several patents.

Prof. Boeck serves at several Technical Program Committees and paper review- and editorial boards of RF- and Microwave Journals. He is a Guest Professor of the Southeast University Nanjing, Nanjing, China, a Senior Member of the IEEE and an international IEEE Distinguished Microwave Lecturer for the years 2006-2008 in the field of "Design of RF CMOS Integrated Circuits".