Petri Net Based Controller Concept For Cognitive Radios in Wireless Access Networks

Alexander Viessmann
University of Duisburg-Essen/Department of Communication Technologies, Duisburg, Germany
Email: alex.viessmann@uni-duisburg-essen.de

Admir Burnic, Christoph Spiegel, Guido H. Bruck and Peter Jung
University of Duisburg-Essen/Department of Communication Technologies, Duisburg, Germany
Email: {admir.burnic, christoph.spiegel, guido.bruck, peter.jung}@kommunikationstechnik.org

Abstract—**This paper will give a detailed discussion about the authors view on Software Defined and Cognitive Radio. After an introduction on different aspects of software radio and a novel approach on cognitive radio is presented. As proof of concept a software defined cognitive radio demonstrator termed Falcon was built up which is described afterwards. The Falcon is entirely based on a modular signal processing concept. In particular, the receiver deploys modules which process and generate log-likelihood ratio (LLR) signals, hence, providing the capability of a plug-and-play-type reconfigurability. To the best knowledge of the authors, such a reconfigurability approach has not yet been pursued as consequently before.**

Index Terms— **Software Defined Radio (SDR), Cognitive Radio (CR), Controller Concept, Petri Net, Reconfigurability**

I. INTRODUCTION

Reconfigurability of transceivers for wireless access networks like Bluetooth, WiMAX (Worldwide Interoperability for Microwave Access) and W-LAN (wireless local area network) will become increasingly important in the forthcoming decade. An appropriately flexible and reliable software architecture, allowing the concurrent processing of different controlling tasks for wireless terminals will hence be an important asset. Since Petri nets (PNs) are both simple and strong tools for the description and the design of such concurrent processes, it is recommendable to deploy them for software defined radio (SDR) and cognitive radio (CR) concepts [1],[2].

Reconfigurability in radio development is not a very novel technique [3]. Already during the 1980s reconfigurable receivers were developed for radio intelligence in the short wave range. However, reconfigurability became familiar to many radio developers with the publication of the special issues on software radios of the IEEE Communication Magazine [4],[5].

The authors in [3] refer to a transceiver as a software radio (SR) if its communication functions are realized as programs running on a suitable processor. Based on the same hardware, different transmitter/receiver algorithms, which usually describe transmission standards, are implemented in software. A SR transceiver comprises all the layers of a communication system, in particular the physical layer, usually abbreviated by PHY layer, and the medium access control layer, denoted by MAC layer.

The baseband signal processing of a digital radio (DR) is invariably implemented on a digital processor. An ideal SR samples the antenna output directly. A software defined radio (SDR) is a practical version of a SR: The received signals are sampled after a suitable band selection filter, usually in the base band or a low intermediate frequency band. One remark concerning the relation between SRs and SDRs is necessary at this point: It is often argued that a SDR is a presently realizable version of a SR because state-of-the-art analog-to-digital converters (ADCs) that can be employed in SRs are not available today. This argument, although it is correct, may lead to the completely wrong conclusion that a SR which directly digitizes the antenna output should be a major goal of future developments. Fact is that the digitization of an unnecessary huge bandwidth filled with many different signals of which only a small part is determined for reception is neither technologically nor commercially desirable.

Hence, there is no reason for a receiver to extremely oversample the desired signals while respecting extraordinary dynamic range requirements for the undesired in-band signals at the same time. Furthermore, the largest portion of the generated digital information, which stems from all undesired in-band signals, is filtered out in the first digital signal processing step.

A cognitive radio (CR) is an SDR that additionally senses its environment, tracks changes, and reacts upon its findings [6]. A CR is an autonomous unit in a communications environment that frequently exchanges information with the networks it is able to access as well as with other CRs. From the authors point of view, a CR is a refined SDR while this again represents a refined DR.

SDR and CR transceivers differ from conventional transceivers by the fact that they can be reconfigured via control units. Such control units need information about the type and standard of the radio communications link

and software modules for the signal processing path in order to reconfigure the receiver properly.

This usually includes a download procedure to obtain some information from the network, the radio communicates with. This download procedure is very vulnerable, because very sensitive data are transferred. An error in the reconfiguration parameters or signal processing software may cause a total malfunction of the SDR. This may include cases where no further reconfiguration is possible due to the fact that no communication to the network is possible anymore because of a disconfigured radio. The reconfiguration has to be a very reliable process for this reason. A side effect of this feature is the possibility to offer a remote diagnosis support for the terminal including remote bug-fixing which could be offered by network operators as well as terminal providers.

In many available publications such as e.g. [7]-[14], more or less inflexible implementation platforms or hardware oriented processing architectures for the control unit have been discussed rather than the software architecture and real-time operation of reliable reconfiguration. In [12] the basic idea of reconfiguration in a wireless environment was addressed. The authors discussed procedures which are relevant to the network and the negotiation process for the updating. However, the software architecture and processing schemes inside terminals were not considered in detail.

II. DEMANDS AND REQUIREMENTS ON COGNITIVE OPERATIONS

Cognitive operation in mobile terminals shall offer at least two major advantages compared to conventional operation. The possibility of reconfigurability leads to the idea of reusing a common hardware for different communication connections and hence allowing smaller, less power consuming and cheaper solutions. In this case, the question which services should be offered simultaneously might limit this advantage of reusing hardware. An example might be a user who is using a 3GPP service and Bluetooth simultaneously with his cell phone. Although it is possible to cover both standards with a common hardware, the demand to offer both services at the same time makes two different systems necessary, where a specialized solution would be most cost effective.

The second advantage of cognitive terminal devices is a more efficient spectrum usage [15]-[17]. Investigations show that the very limited and expensive resource "frequency spectrum" is used very inefficiently [18]. Due to the ability of monitoring the spectrum, cognitive radio terminals are able to dynamically reallocate bandwidth for different purposes.

Cognitive radio terminals will be able to realize true choices with "pay as you go" features and offer device independence with a single piece of scalable hardware that is at once compatible at a global extent. Network operators will be able to differentiate their service offerings without having to support a myriad number of handhelds. They can move to adjacent markets as well as offer new, tiered services to increase their revenue mix. Infrastructure suppliers will participate in the opportunity to lower cost and insure themselves against price erosions though concentrated efforts on a common hardware

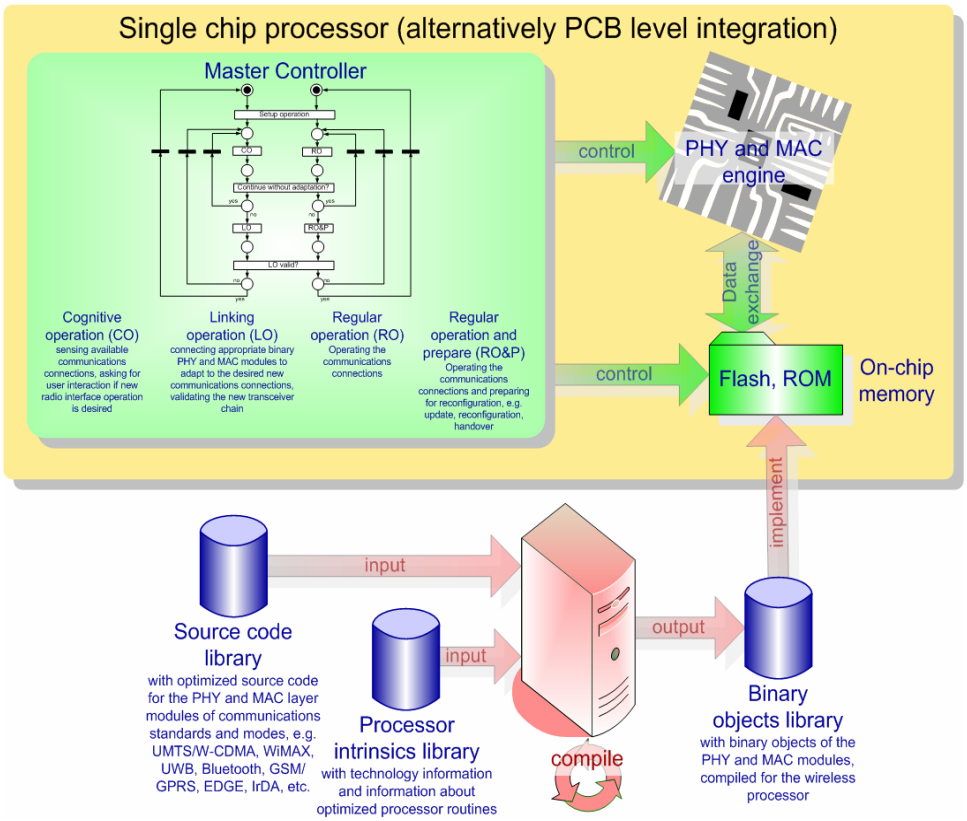

Figure 1: Concept of the master controller for reliable reconfiguration of CRs

platform and reduced component counts. Application developers will be able to enhance the value without concern to hardware types. Terminals providers are able to add features, patches and capabilities to devices for broader market participation.

The tasks that have to be solved can be distinguished between the analog and digital domain. The digital part should be reconfigurable i.e. software defined by definition, contain DSP core(s) for PHY (physical) layer signal processing and contain microcontroller(s) for MAC (medium access control) layer and higher OSI (Open Systems Interconnection) layer processing and common controlling purposes. Of course, SDR/CR terminals might contain FPGA(s) (field programmable gate arrays), however the reconfiguration becomes cumbersome in this case and a DSP based solution is suggested by the authors and will be presented in chapter IV.

The analog part provides variable carrier frequencies and bandwidths in the radio frequency (RF) domain in order to meet the frequency regulation constraints of different countries. Furthermore, tunable low-pass filters for baseband filtering have to be implemented here. The ADC/DAC clocks have to support varying sampling rates to prevent the need for fractional decimation algorithms due to different channel bandwidths or symbol clocks. The RF-frontend should support a low noise amplification in up- and down conversion capabilities.

The criteria which are imposed by the view on different communication standards are the frequency range, the system and channel bandwidths and the channel raster. The channel raster is usually regulated, and many countries and standards follow the ETSI (European Telecommunications Standards Institute) recommendations [19]. An important limitation for reuse of analog components is the input power, i.e. the sensitivity of the device and the maximum output power which varies drastically. Different modulation schemes impose different effects of analog impairments on the signal quality which also limit the reuse of analog components. As aforementioned, the concurrent processing of different standards will be an important asset for future cognitive radio terminal implementations. While offering all these services to the users, the power consumption of the device should be as low as possible because of the rigorous demand on mobility for future terminals.

To meet the specification of different standards, the terminal has to support varying multiple access schemes like FDMA, TDMA, CDMA and SDMA (frequency, time, code and spatial division multiple access). This has an impact on the analog circuitry, too. Several modulation schemes have to be supported which could make special hardware accelerators necessary. An example would be a FFT (fast Fourier transform) coprocessor for OFDM (orthogonal frequency division multiplex) based communication. Analog impairments like I/Q (Inphase/Quadrature) imbalances and frequency errors have to be compensated digitally. Especially the spectrum monitoring needed for cognitive operation makes the implementation of highly sophisticated digital spectral analysis algorithms mandatory like suggested in [20], [21] and [22], respectively. A solution based on iterative frequency sensing will be described in the following.

III. Iterative Frequency Sensing method

As discussed before, cognitive operation in a mobile terminal requires a frequency or a network sensing capability, by means of sensing for available wireless services and systems which can potentially provide service to user equipment. Because of these reasons, frequency sensing is one of the most important issues in cognitive radio. Frequency sensing must be accomplished seamlessly and repeatedly at the user equipment. The implementation has to be done very efficiently to require lowest implementation complexity and to run with the lowest possible power consumption. Hence, an iterative method is recommendable.

User equipment for cognitive radio applications is inherently multistandard/multimode capable. In such user equipment, all frequency bands potentially being allocated to systems and modes which the user equipment can connect to, must be scanned and the available standards and modes must be identified. This scanning of the frequency bands can be done continuously, i.e. persistently which implies dedicated RF-hardware which delivers information about changes in network services immediately. The scanning process could also be implemented discontinuously, i.e. non-persistently, which does not necessarily require dedicated hardware but has the disadvantage of an increased reaction time in the system until changes are recognized.

In the case of a successful recognition the offered services must be identified and the result must be ranked with respect to the provided service classes and the available and offered QOS (quality of service) e.g. based on rate, delay, BLER (block error ratio) and received signal strength. According to this ranking, possible candidate networks providing services to the terminal are identified and user interaction has to be considered, too.

Conventional terminal implementations basically strive for the evaluation of a single standard and single mode at a time. The mode of operation is based on the detection of the radio beacon e.g. BCCH (Broadcast Control Channel) in GSM (Global System for Mobile Communications) terminology associated with a particular standard, including coarse and fine frequency acquisition and cell selection by frame and slot synchronization. To the best knowledge of the authors, decisions made on the available modes or even multiple standards have not been considered yet. An extension of existing algorithms is therefore required to formulate a novel strategy.

The proposed method is user equipment oriented or mobile originated in GSM terminology. This operational step will be included in the cognitive operation of the master controller, which will be described in chapter IV. The implementation of frequency sensing can be done centrically in analog domain, digital domain or mixed

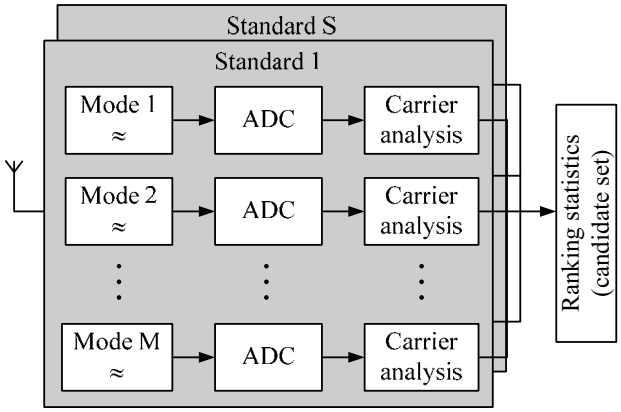

Figure 2: Frequency sensing method in parallel configuration

mode. The algorithm could be implemented in an all parallel version or an all sequential version. The first case is illustrated in Fig. 2.

The proposed carrier analysis evaluates the energy/power within each carrier and ranks the carriers according to their power. For each mode, the carrier has to be synchronized according to its rank and available service parameters have to be evaluated. A simplification or reduction of complexity could be accomplished by just evaluating the strongest carrier per mode or the ranking of the *Z* strongest carriers over all modes and standards only.

In the following, an appropriate algorithm for UMTS type services is proposed. To demodulate W-CDMA (wideband CDMA) signals, a tap amplitude and delay estimation (TADE) algorithm is necessary. Up to now, TADE algorithms are such complex that it is not feasible to deploy them in RISC processors or DSPs. A favorable TADE algorithm termed correlation based iterative TADE(CITADE) will be presented in the following. The proposed algorithm has a low complexity with minimal performance sacrifices.

CITADE uses the Primary Synchronization Code (PSC) of UMTS/W-CDMA. The PSC consists of a unique CDMA code based on a generalized hierarchical Golay sequence. The Q real valued code elements c_q are converted to complex-valued elements $\underline{c}_q$ by multiplication with $\exp\{j\pi/4\}$:

$$\underline{c}_q = \exp\{j\pi/4\}\, c_q \tag{1}$$

The resulting complex signal $\underline{c}(t)$ is formed by

$$\underline{c}(t) = \sum_{q=1}^{Q} \underline{c}_q \delta\left(t - [q-1]T_c\right) \tag{2}$$

Prior to transmission the signal is filtered by a transmit filter. The TX filter has a root raised cosine characteristicwith a roll-off factor of α = 0.22.

The reference signal $s(t)$ is transmitted over a mobile radio channel. The channel with P paths is assumed stationary during transmission of reference signal. To the receive signal zero-mean white Gaussian noise is added. The received signal is filtered with the RX filter, which has the same characteristic as the TX filter. The concatenation of the TX and RX filters results in the raised-cosine (RC) characteristic.

$$\begin{aligned} h_{\mathrm{RC}}(t) &= h_{\mathrm{RRC}}(t) * h_{\mathrm{RRC}}(t) \\ &= \frac{\sin\left(\pi \frac{\tau}{T_c}\right)}{\pi \frac{\tau}{T_c}} \cdot \frac{\cos\left(\alpha\pi \frac{\tau}{T_c}\right)}{1-\left(2\alpha \frac{\tau}{T_c}\right)^2} \end{aligned} \tag{3}$$

TADE is part of the transmission chain as can be seen in Figure 3. The signals are sampled with rate 1/Ts. The amplitude and the delay of taps are estimated and the results are provided to further signal processing instances, e.g. RAKE receiver.

Sampled signals can be written in vector-matrix notation. To do this the received signal is sampled and stored in the vector:

$$\underline{\boldsymbol{r}} = \left(\underline{r}_1 \quad \underline{r}_2 \quad \cdots \quad \underline{r}_{N_s Q + N_s N_w - N_s}\right)^{\mathrm{T}} \tag{4}$$

Sampling the effective channel impulse response and the noise the same way yields

$$\underline{\boldsymbol{b}} = \left(\underline{b}_1 \quad \underline{b}_2 \quad \cdots \quad \underline{b}_W\right)^{\mathrm{T}}, \tag{5}$$

$$\underline{\boldsymbol{n}} = \left(\underline{n}_1 \quad \underline{n}_2 \quad \cdots \quad \underline{n}_{N_s Q + N_s N_w - N_s}\right)^{\mathrm{T}} \tag{6}$$

Now the received vector $\boldsymbol{r}$ can be expressed as:

$$\underline{\boldsymbol{r}} = \underline{\boldsymbol{C}}\underline{\boldsymbol{b}} + \underline{\boldsymbol{n}} \tag{7}$$

with $\underline{\boldsymbol{C}}$ being a convolution matrix holding the complex valued PSC elements. N_s shall be the length of oversampled correlation sequence and $W = N_s N_w$ shall be the length of oversampled channel impulse response.

The received signal can be separated in N_s distinct sets of samples:

$$\underline{\boldsymbol{r}}^{(n_s)} = \left(\underline{r}_{n_s} \quad \underline{r}_{n_s + N_s} \quad \cdots \quad \underline{r}_{n_s + N_s (Q + N_w - 2)}\right)^{\mathrm{T}} \tag{8}$$

with $n_s = 1 \ldots N_s$.

With appropriate definitions for the effective channel response $\underline{\boldsymbol{b}}^{(n_s)}$ and the noise vector $\underline{\boldsymbol{n}}^{(n_s)}$ the received signal vector is written as

$$\underline{\boldsymbol{r}}^{(n_s)} = \underline{\tilde{\boldsymbol{C}}}\,\underline{\boldsymbol{b}}^{(n_s)} + \underline{\boldsymbol{n}}^{(n_s)}, \quad n_s = 1 \ldots N_s \underline{\boldsymbol{n}}^{(n_s)} \tag{9}$$

with $\underline{\tilde{\boldsymbol{C}}}$ being a sub-matrix of $\underline{\boldsymbol{C}}$, where

$$\underline{\boldsymbol{C}} = \underline{\tilde{\boldsymbol{C}}} \otimes \boldsymbol{I}_{N_s}, \quad \underline{\tilde{\boldsymbol{C}}} = \exp\{j\pi/4\}\,\tilde{\boldsymbol{C}} \tag{10}$$

$\otimes$ denotes to the Kronecker product.

Thus the proposed algorithm can be summarized:

1. Estimate the undersampled effective channel impulse responses $\hat{\underline{\boldsymbol{b}}}^{(n_s)}$ of $\underline{\boldsymbol{b}}^{(n_s)}$ by using a correlative estimator:

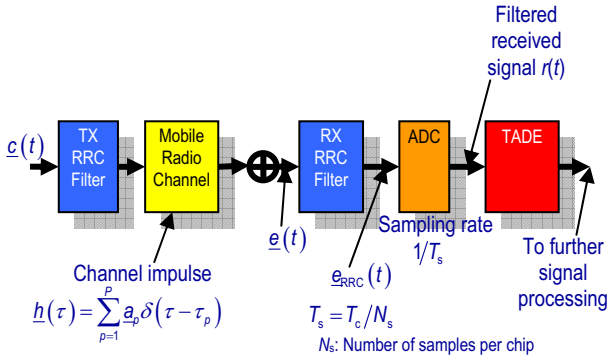

Figure 3: Tade in transmission scheme

$$\hat{\underline{\boldsymbol{b}}}^{(n_s)} = \frac{1}{E_c}\tilde{\underline{\boldsymbol{C}}}^{\mathrm{H}}\boldsymbol{r}^{(n_s)} = \frac{\exp\{-\mathrm{j}\pi/4\}}{Q}\tilde{\boldsymbol{C}}^{\mathrm{T}}\boldsymbol{r}^{(n_s)} \qquad (11)$$

with $n_s = 1 \ldots N_s$.

2. Sort the elements of all N_s effective channel impulse response vectors according to decreasing energy $\left|\hat{\underline{b}}_{\nu(p)}\right|^2$. Denote the indices with $\nu(p)$, $\nu(p) \in \mathbb{N}$, $1 \le \nu(p) \le W$. These form the estimates of the amplitudes of the channel impulse response:

$$\begin{aligned}\hat{\underline{\boldsymbol{a}}} &= \left(\hat{\underline{a}}_1 \quad \hat{\underline{a}}_1 \quad \cdots \quad \hat{\underline{a}}_P\right)^{\mathrm{T}} \\ &= \left(\hat{b}_{\nu(1)} \quad \hat{b}_{\nu(1)} \quad \cdots \quad \hat{b}_{\nu(P)}\right)^{\mathrm{T}}\end{aligned} \qquad (12)$$

3. Determine the corresponding delays according to:

$$\begin{aligned}\hat{\boldsymbol{\tau}} &= \left(\hat{\tau}_1 \quad \hat{\tau}_2 \quad \cdots \quad \hat{\tau}_P\right) \\ &= \left(\left[\nu(1)-1\right]T_s - \frac{T_{RC}}{2} \cdots \left[\nu(P)-1\right]T_s - \frac{T_{RC}}{2}\right)\end{aligned} \qquad (13)$$

The proposed CITADE algorithm was implemented on the TI C6416 platform as proof of concept and is part of the master controller, which will be described in the following.

IV. Petri Net Based Master Controller

The way of reconfiguring the terminal, in particular the realization of a processor with master controller and a Petri net based approach, which allows concurrent mode of operation, high reliability and secure applications, has not yet been treated. In this communication, the authors propose a viable and new approach for such a reconfiguration. The new approach consists of a master controller which is responsible for a reliable reconfiguration. In addition, there has to be a unit, which can communicate with the network, a PHY and MAC engine. This PHY and MAC engine needs software modules with signal processing algorithms for the data processing path. The third part is a memory, which contains these software modules. The master controller starts a cognitive operation in order to obtain the best reconfiguration and software modules needed for the SDR.

The reconfiguration then consists of linking software modules existing in the memory, and installing them into the SDR to use the software modules in the regular signal processing chain. The master controller works with Petri net based software architecture. It needs a scalable control program by using e.g. Petri net compilers. The implementation and validation of the master controller based concept on a PCB level integration will be done by setting out from currently used demonstrator platforms. It will be implemented in a single chip processor after validation of the PCB level integration.

The key component is the concept of the master controller including the appropriate Petri net based controlling schemes. Some anticipated concurrent tasks are shown in Fig.1, namely the linking operation, the cognitive operation and the regular operation.

After power on reset, the master controller starts a setup operation. The parameters and software modules for the last used wireless communication standard are then loaded from the single chip processor's on-chip memory into its PHY and MAC engine, which is then the ready to communicate using the wireless communication standards. Then, the regular operation (RO) is started, which operates the communication connections of the device. During the setup operation, the Cognitive operation (CO) is prepared. It operates at the same time as the RO, but it senses for available communication connections. If it has been successful in perceiving a new connection, it asks for user interaction, if the new radio interface operation is desired. The user interaction may be skipped, if the user has allowed this.

In case of a reconfiguration to take place, the linking operation (LO) is started. It connects appropriate binary PHY and MAC modules in order to adapt to the desired new communications connections and it validates the new transceiver chain. At the same time, the regular operation & prepare (RO&P) prepares the system for reconfiguration, e.g. update, reconfiguration and handover, while operating the communication connections at the same time.

The validation of the linked modules is necessary to avoid conflicts which may arise when the linked signal processing path is not able to work properly with the new wireless communications standard and to increase reliability. A complete malfunction of the device may be possible, if no such validation is made. In case of a negative validation, the RO and CO start again as before. No change will be done in the signal processing path. In case of a positive validation a new setup process starts, which reconfigures the SDR starting the RO and CO including the new signal processing path for the newly adapted wireless communications link.

The master controller is Petri net based to simplify the software design, which leads to a better service quality of the controller. Main part of the whole system is the PHY and MAC engine, which runs the software modules for

the different wireless modes and standards. It contains a processor for the digital signal processing.

The software modules must be validated with such a PHY and MAC engine before they are released for use in devices by storing them into the memory. A first device to test the suggested method is a software defined radio demonstrator, which will be introduced in the next section.

V. Demonstrator Design

A cognitive radio demonstrator should support at least two standards in order to show the reconfigurability. The complete communication chain has to be included, i.e. the digital baseband MAC and PHY layer processing, the analog baseband and intermediate frequency functions like filtering, ADC and DAC with varying samplings rates, mixing, amplification and radio frequency frontend functions like e.g. up- and down-conversion. It should be a reconfigurable i.e. software defined solution for the PHY and MAC layer processing and it should able to process all standards in real-time. In addition, it should support a spectrum monitoring capability by definition.

For demonstration purposes of the presented concept the authors implemented a demonstrator termed Falcon. The Falcon currently consists of two identical transceivers (TRXs).

Fig. 4 shows a photograph of one of these TRXs. Each TRX consists of an RF front-end board with a single 802.11bg direct down-conversion RF chip, provided by Atmel, an analog TRX baseband board with filtering and signal conversion parts and a SPI (serial peripheral interface) for the DSP based programming of the RF chip, the mixed signal board carrying the ADC (analog-to-digital converter) and DAC (digital-to-analog converter) hardware, a programmable PLL in order to offer different sampling rates, a USB (universal serial bus) interface board for transfering the information to the transmitter and the detected information to the sink, and a TMS320C6416 DSP starter kit (DSK), provided by Texas Instruments (TI), with a joint test action group (JTAG)

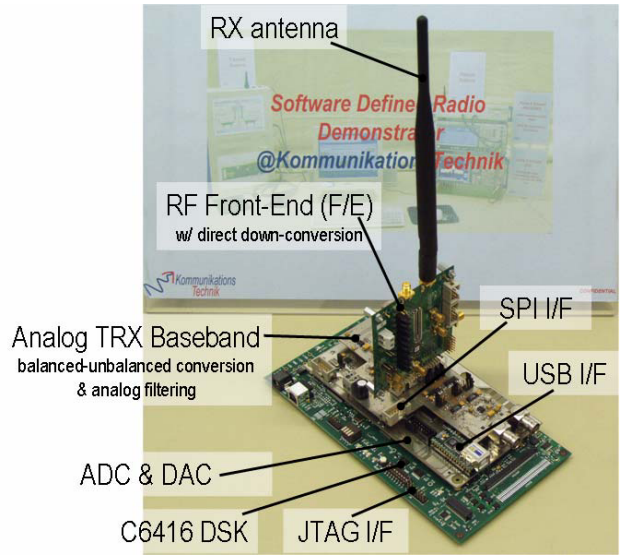

Figure 4: Falcon transceiver

interface for controlling and programming purposes. The RF frontend board can provide transmit power values ranging from −26 dBm to −14 dBm without further power amplification and they have separate transmit and receive antenna connectors; in Fig. 3, only the receive antenna is connected. The frontend is designed for W-LAN 802.11bg originally, with a local oscillator being located at 2.4 – 2.484 GHz. The 3GPP services are demonstrated using this frequency band too, although frequency regulation provides different bands. This is done in the experimental laboratory setup to show the feasibility of the concept.

The hardware/software integration has been done in the authors' laboratory as well as the development of all signal processing modules, which have been realized in C language tailored for the TMS320C6416 DSPs.

Currently, UTRA W-CDMA 384 kbps and WiMAX 802.16e are implemented in the demonstrator. The demodulation component for W-CDMA contains the RF receive part, the RRC (root raise cosine) filtering, the adaptive rake receiver consisting of a searcher exploiting the synchronization channels for frame and slot synchronization as well as channel parameters identification and rake finger allocation, a variable number of adaptive rake fingers including the channel parameter tracking, the de-scrambling and the de-spreading, a maximal-ratio combining (MRC) unit including a signal-to-interference-and-noise ratio (SINR) estimation unit, a parallel-to-serial conversion unit, a LLR (log likelihood ratio) computation unit, and, finally, the frame and slot disassembling.

Fig. 5 gives a general overview of communication systems. After removing irrelevance and redundancy during the source coding process, the chanel coding adds redundancy systematically for error recognition and correction in the receiver. After modulation, the signal is transmitted via a radio channel and noise is added at the receiver side in this model. At the receiver side, the signal passes the communication chain in a reversed order. The signal demodulation quality can be improved by using a-priori knowledge iteratively. This leads to an implementation based on the usage of reliability information, e.g. in form of LLRs [23].

In the case of the 3GPP services, the channel decoding component shown in Fig.5 consists of the second de-interleaving, the radio frame and the physical channel de-segmentation, the first de-interleaving, the Turbo decoding with rate de-matching, and the CRC (cyclic redundancy check) verification.

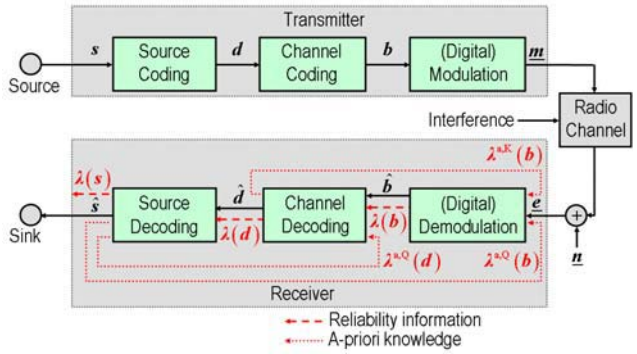

Figure 5: Basic discrete-time structure of a digital radio communication system with a modular iterative receiver, cf.[23], Fig. 1.4, p. 11

VI. Measurement Results

In this section, several measurement results obtained with the Falcon for the UTRA (UMTS Terrestrical Radio Access)-FDD (frequency division duplex) 384 kbit/s service will be presented. The obtained measurement results will be compared to system simulations based on a W-CDMA simulator and a channel model developed at the authors' department. The main criteria during this investigation are BER (bit error ratio) and BLER. In addition, transmit and receive front-end characteristics will be considered. Finally, the results of a sensitivity measurement will be presented and an overview of the signal processing complexity will be given. Fig. 5 shows the eye diagrams of the in-phase and quadrature signals at the baseband input of the RF front-end chip for the UTRA FDD 384 kbit/s service.

No pilot transmission has been considered which is the reason for the occurrence of amplitude values around zero.

The measured values of the error vector magnitude (EVM) at the input of the transmit antenna versus the transmit power are shown in Fig. 7.

According to that, the EVM ranges between 7% and 8% for transmit power values between -26 dBm to -17 dBm. Only in the case of high transmit power values

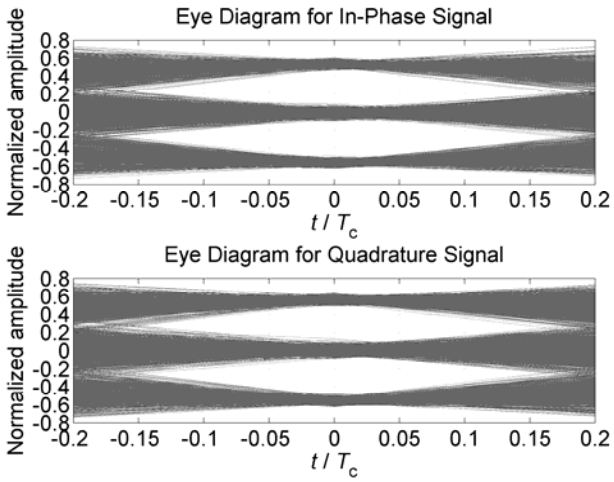

Figure 6: Eye diagrams of the in-phase and quadrature signals at the input of the RF board

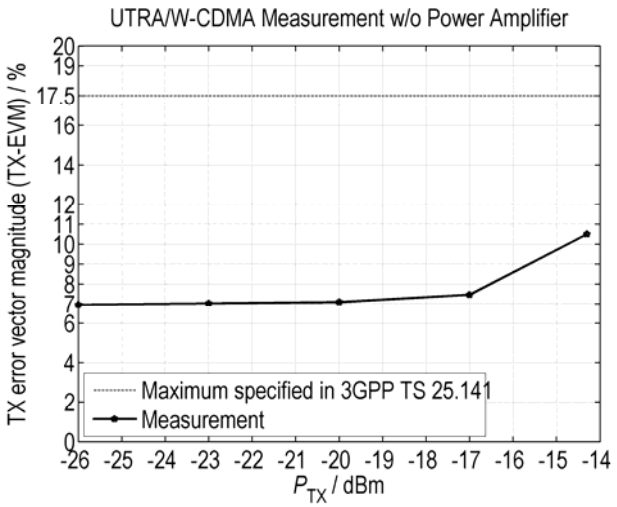

Figure 7: Measured error vector magnitude values at the transmitter output

above -17 dBm, the EVM increases to approximately 10.5%. In all cases the EVM is well below the maximum allowed EVM of 17.5%, specified in the UMTS standard.

Fig. 8 shows obtained simulation and measurement results for the UTRA FDD 384 kbit/s service in the case of the transmission over the 3GPP Test Case 4 channel model which has been implemented in a channel simulator.

The simulations were carried out with a floating point implementation of the signal processing algorithms implemented in C language. The measurements have been done with the digital implementation of the Falcon, the mixed signal and RF parts have not been considered.

The simulator determines the matched filter BER bound, which is the best possible performance in case of the transmitting isolated bits over the channel and perfect knowledge about the channel at the receiver, together with the uncoded BER which can be obtained when considering the UTRA FDD 384 kbit/s service. The latter is of course worse than the matched filter bound. Furthermore, the simulator computes the BER and the BLER at the output of the Turbo decoder. For reference purposes, we will consider the coded BER 10^{-4} and the

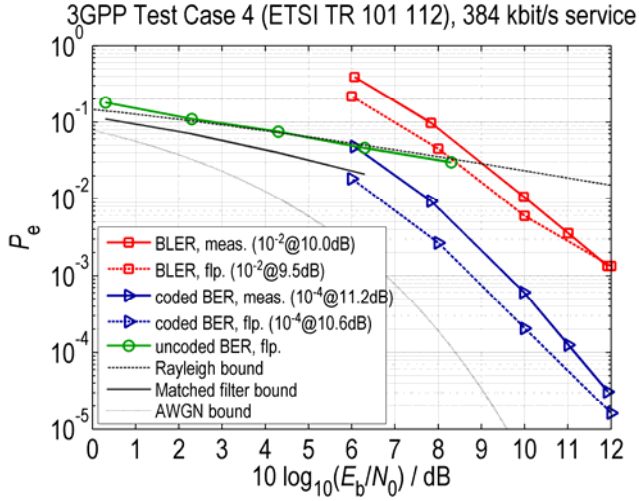

Figure 8: Comparison of performance measurements and simulation results in the case of the 3GPP Test Case 4 channel model described in ETSI TR 101 112 for the 384 kbit/s service

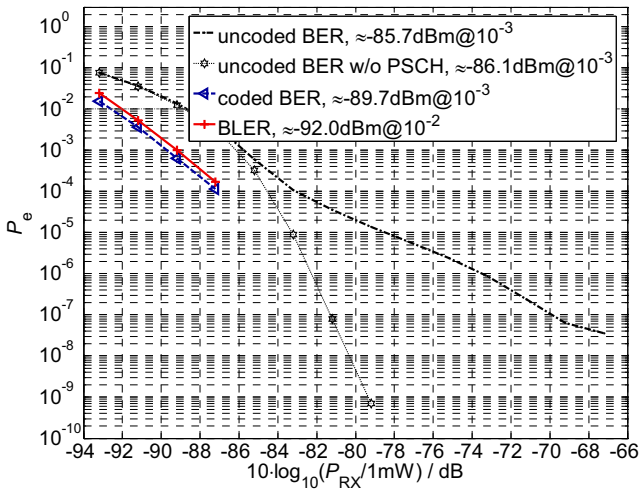

Figure 9: Falcon receiver sensitivity measurement in 3GPP 384 kBit/s service configuration

coded BLER 10^{-2}, the latter meaning that 99% of all transmitted blocks have been received correctly, i.e. the throughput is equal to 99% if no ARQ is considered. In the case of the 3GPP Test Case 4 channel, we require ≈10.6 dB to achieve the coded BER of $10^{-4}$and ≈10.6 dB to obtain the coded BLER of 10^{-2}. The fixed point implementation in the Falcon causes a small degradation of approximately 0.5 dB, and we yield ≈11.2 dB to achieve the coded BER of 10^{-4} and ≈10.0 dB to obtain the coded BLER of 10^{-2}.

Fig. 9 shows the results of the sensitivity measurement of the 384 kBit/s 3GPP service. It shows the BER probability depending on the receiver input power.

The uncoded BER shows performance degradation in the case of high input power and hence large signal to noise ratio. The reason of this effect is the PSCH not being perfectly orthogonal to the data channel. Because of this, the BER is calculated in a region where only the data channel occurs, in a second curve. The curve shows the behavior which is expected from theory for a QPSK scheme very well. The measurement shows an uncoded BER performance of 10^{-3} at input powers of -85.7 dBm and -86.1 dBm in the case of adjusted PSCH, respectively.

The coded BER measurement shows a performance of 10^{-3} at a receiver input power of -89.7 dBm and a BLER of 10^{-2} at -92.0 dBm , which is considered as the minimum requirement for voice based services. The channel code which was deployed was a Turbo code with code rate 1/3. At input powers larger than -87 dBm the demonstrator does not show any bit errors in the case of coded transmission.

The sensitivity of the Falcon transceiver is limited by the 802.11bg frontend which is used in the demonstrator. WLAN services do not specify as large receiver sensitivity as 3GPP does.

As aforementioned, the implementation is running on TI C6416 DSP at 1 GHz clock. Table 1 gives an overview of the signal processing complexity in terms of a percentile of the available computing time.

Table 1: Signal processing time for UTRA FDD 384 kBit/s service in fixed point implementation

Receiver fixed point module	Percentile CPU load
Rake finger incl. adpaptive frequency tracking	≈ 54
Complex low pass filter (RRC)	≈ 11
PSCH correlation	≈ 9
LLR calculation, deinterleaving	≈ 7
DC cancellation	≈ 2
AGC	≈ 0.3
SSCH correlation (frame-synchronization)	≈ 0.1
Turbo decoding (co-processor preparation)	≈ 0.1
CRC16	≈ 0.1
DCCH processing	<< 1
Channel acquisition (done once at startup)	0 / 33

Most of the processing time is needed by the adaptive rake finger which additionally implements an adaptive frequency tracking algorithm and hence compensates for the frequency errors in the TRX local oscillators. One has to note that the low processing time which is necessary for Turbo decoding can be achieved by using the turbo code coprocessor of the TI C6416 device only. The channel acquisition is only done once on startup, leading to no processor load during regular operation. During this time, around 33% processing time is consumed.

ACKNOWLEDGMENT

The authors wish to thank Atmel Duisburg GmbH and Texas Instruments for their generous support. Finally, they gratefully acknowledge the support of their colleagues at the Lehrstuhl für KommunikationsTechnik at the Duisburg-Essen University.

REFERENCES

[1] R. David, H. Alla: *Discrete, Continous, and Hybrid Petri Nets*, Springer, Berlin, Heidelberg, 2005

[2] J. Billington, M. Diaz, G. Rozenberg : *Application of Petri Nets to Communication Networks*, Springer, Berlin, Heidelberg, 1999

[3] F.K. Jondral, *Software-defined radio – basics and evolution to cognitive radio*, EURASIP Journal on Wireless Communications and Networking, vol. 3 (2005), pp. 275-283, including all references.

[4] Various authors, *Special Issue on software radio*. IEEE Communications Magazine, vol. 33 (May 1995), issue 5.

[5] Various authors, *Special Issue on globalization of software radio,* IEEE Communications Magazine, vol. 37 (Feb. 1999), issue 2.

[6] J. Mitola, *Cognitive Radio - An Integrated Agent Architecture for Software Defined Radio*, Dissertation, Royal Institute of Technology, Kista, Sweden, 2000
[7] S. Srikanteswara; J.H. Reed, P. Athanas; R. Boyle, *A soft radio architecture for reconfigurable platforms*, IEEE Communications Magazine, vol. 38 (Feb. 2000), Issue 2, pp. 140 – 147,
[8] M. Laddomada; F. Daneshgaran; M. Mondin; R.M. Hickling, *A PC-based software receiver using a novel front-end technology*, IEEE Communications Magazine, vol. 39 (Aug. 2001), Issue 8, pp. 136 – 145
[9] J. Glossner, D. Iancu; J. Lu; E. Hokenek; M. Moudgill, *A software-defined communications baseband design*, IEEE Communications Magazine, vol. 41 (January 2003), Issue 1, pp. 120 – 128.
[10] S. Srikanteswara; R.C. Palat; J.H. Reed; P. Athanas, *An overview of configurable computing machines for software radio handsets*, IEEE Communications Magazine, vol. 41 (July 2003), Issue 7, pp. 134 – 141.
[11] N.J. Drew; M.M. Dillinger, *Evolution toward reconfigurable user equipment*, IEEE Communications Magazine, vol. 39 (Feb. 2001), Issue 2, pp. 158 – 164.
[12] M. Mehta; N. Drew; C. Niedermeier, *Reconfigurable terminals: An overview of architectural solutions* IEEE Communications Magazine, vol. 39 (Aug. 2001), Issue 8, pp. 82 – 89.
[13] J. Palicot; C. Roland, *A new concept for wireless reconfigurable receivers*, IEEE Communications Magazine, vol. 41 (July 2003), Issue 7, pp. 124 – 132.
[14] J. Hoffmeyer; I.-P. Park; M. Majmundar, S. Blust, *Radio software download for commercial wireless reconfigurable devices*, IEEE Radio Communications, March 2004, pp. S26-S32.
[15] Čabrić D., Mishra S. , Willkomm D., Brodersen R., Wolisz A.: *A Cognitive Radio Approach for Usage of Virtual Unlicensed Spectrum*, Proceedings. of 14th IST Mobile Wireless Communications Summit 2005, Dresden, Germany, June 2005
[16] R. W. Brodersen, A. Wolisz, D. Cabric, S. M. Mishra, D. Willkomm, *CORVUS: A Cognitive Radio Approach for Usage of Virtual Unlicensed Spectrum*, University of California, Berkley, 2004
[17] A. Ginsberg, J.D. Poston, and W:D. Horne: *Experiments in Cognitive Radio and Dynamic Spectrum Access using An Ontology-Rule Hybrid Architecture*, Second international conference on Rules and Rule Markup Languages for the semantic Web, November 2006, Georgia USA
[18] M. A. McHenry: *NSF Spectrum Occupancy Measurements Project Summary*, Shared Spectrum Company 1595 Spring Hill Road, Suite 110 Vienna, VA 22182, www.sharedspectrum.com
[19] ETSI: Final draft ETSI EN 301 021 V1.6.1, ETSI 650 Route des Lucioles, F-06921 Sophia Antipolis Cedex – France, 2003
[20] D. Cabric; S.M. Mishra, R.W. Brodersen: *Implementation Issues in Spectrum Sensing for Cognitive Radios*, Conference Record of the Thirty-Eighth Asilo-mar Conference on Signals, Systems and Computers, 2004, Volume 1, Date: 7-10 November 2004, pp 772 - 776 Vol.1
[21] W.A. Gardner: *Signal Interception: A Unifying Theoretical Framework for Feature Detection*, IEEE Transactions on Communications, Vol. 36, No. 8, August 1988
[22] S.L. Marple Jr.: *Digital Spectral Analysis with applications*, Prentice-Hall Signal Processing Series, Englewood Cliffs, New Jersey, 1987
[23] T. Faber, *Turbo-Empfänger für digitale Mobilfunksysteme, gezeigt am Beispiel eines "Software Defined Radio"-Demonstrators*, Series "Selected Topics in Communications Technologies," (edited by Prof. Dr.-Ing. habil. Peter Jung), Aachen: Shaker, 2005.

Alexander Viessmann was born in Krefeld, Germany in 1978 and began his studies in electrical engineering in 1999 at the former Gerhard-Mercator-University of Duisburg and pursued his studies in the field of microelectronics. Alexander Viessmann obtained the diploma degree in electrical engineering (M.Sc. EE equivalent) in 2005 from the department of electrical engineering at the university of Duisburg-Essen, Duisburg, Germany.

He joined the RF division of Atmel and the Chair of Communication Technologies at Duisburg-Essen University in 2005. He is working towards his Ph.D. in the field of innovative reconfigurable wireless communication technologies. Further research interests are oscillator and PLL design.

Mr. Viessmann received the Siemens Siemens Communications Academic Award for his diploma thesis in the field of oscillator design in 2005 and the Texas Instruments Excellence in Signal Processing Award in 2006. In addition, Mr. Viessmann is co-recipient of the Gerotron EEEfCOM innovation award, category universities, 2006.

Admir Burnic was born in Sanski-Most, Bosnien-Herzegowina in 1969. He studied electrical engineering at the Gerhard-Mercator-University Duisburg from 1994 until 2001 and received his diploma degree (M.Sc.EE equiv.) in June 2001. From July 2001 until June 2003, he was with the Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS), Duisburg, working in the field of UTRA FDD performance evaluation. Since July 2003, he has been with the Department of Communication Technologies at the Universität Duisburg-Essen as a Ph.D. candidate. His main focus is UTRA FDD, joint transmission and irregular sampling.

Mr. Burnic received the Texas Instruments Excellence in Signal Processing Award in 2006 and is co-recipient of the Gerotron EEEfCOM innovation award, category universities, 2006.

Christoph Spiegel was born in Oberhausen, Germany in 1980 and began his studies in electrical and information engineering in 2000 at the former Gerhard-Mercator-University, Duisburg, Germany. Later on, he delved into the field of communications. Christoph Spiegel received the diploma degree in electrical engineering (M.Sc. EE equivalent) in 2005 from the department of electrical engineering at the Duisburg-Essen University, Duisburg, Germany.

In 2006, he joined the department of Communication Technologies at the Duisburg-Essen University as a Ph.D. student. His major research topics focus on 4G radio and irregular sampling techniques.

Mr. Spiegel is IEEE member and committed to the local student branch. Mr. Spiegel received the Siemens Communications Academic Award as well as the University Award and the Atmel Award for his diploma thesis in the field of irregular sampling. Moreover, Mr. Spiegel received the Texas Instruments Excellence in Signal Processing Award and

is also co-recipient of the Gerotron EEEfCOM Innovation Award 2006.

Guido H. Bruck, was born in Düsseldorf, Germany on July 3, 1958, studied electrical and electronics engineering and received the Diplom-Ingenieur (M.Sc. EE equivalent) degree at the Universität Duisburg, Germany in 1984. He received the Dr.-Ing. degree from the Universität Duisburg, Germany in 1989.

He joined the Department of Communication Equipment and Systems at the Universität Duisburg, Germany in 1984. Since 2000 he is as a senior engineer with the Department for Communication Technologies at the Universität Duisburg, Germany. He worked in the field of source coding of video signals. His main research areas are multimedia applications, Quality of Service for mobile communications and Software Defined Radio.

Dr. Bruck received the Texas Instruments: ESPA - Excellence in Signal Processing Award in 2006..

Peter Jung (S'91-M'92–SM'96) received the the diploma (M.Sc. equiv.) in physics from University of Kaiserslautern, Germany, in 1990, and the Dr.-Ing. (Ph.D.EE equiv.) and Dr.-Ing. habil. (D.Sc.EE equiv.), both in electrical engineering with focus on microelectronics and communications technology, from University of Kaiserslautern in 1993 and 1996, respectively. In 1996, he became private educator (equiv. to reader) at University of Kaiserslautern and in 1998 also at Technical University of Dresden, Germany.

From March 1998 till May 2000 he was with Siemens AG, Bereich Halbleiter, now Infineon Technologies, as Director of Cellular Innovation and later Senior Director of Concept Engineering Wireless Baseband. In June 2000, he became Full Professor and Chair for Communication Technologies at Gerhard-Mercator-University Duisburg. This university was merged to the Universität Duisburg-Essen at Duisburg, Germany in 2003. His areas of interest include wireless communication technology, software defined radio, and system-on-a-chip integration of communication systems.

Prof. Dr.-Ing. habil. Jung was co-recipient of the best paper award at the ITG-Fachtagung Mobile Kommunikation, Ulm, Germany, in 1995, and he was co-recipient of the Johann-Philipp-Reis-Award for his work on multicarrier CDMA mobile radio systems in 1997.