A CMOS Analog Front-end Receiver with Desensitization to Input Capacitance for Broadband Optical Wireless Communication

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***Abstract*—Line-of-sight optical wireless channels are emerging as a promising broadband wireless access technology. This paper describes a front-end transimpedance amplifier (TIA) that is designed to overcome challenges faced by high-speed optical wireless links requiring receivers with wide field-of-view (FOV) and high dynamic range for signal acquisition/tracking. This transimpedance amplifier employs a capacitive feedback configuration, with a self-biased automatic gain control (AGC) circuit to increase the input dynamic range. The transimpedance amplifier is designed for integration with wide FOV detectors with associated capacitance up to 5pF and its performance is insensitive (within 5%) to an order of magnitude variation in input capacitance. The self-biased AGC allows 42dB dynamic range in received optical power to accommodate varying link ranges and different optical wireless (OW) system configurations. A test chip was implemented in a low-cost 0.5-μm CMOS process and achieves a maximum TIA gain of 52dBΩ , -3dB bandwidth of 523MHz at 5pF input capacitance, and variable TIA gain from 52dBΩ to 36dBΩ without instability. Noise measurements show input-referred noise current spectral density of 22pA/$\sqrt{}$Hz for 5pF input capacitance. Optical measurements show good eye diagrams at 750Mb/s. The power dissipation is 53mW from dual 3.3V and 1.8V supply voltages.**

***Index Terms*—transimpedance amplifier, CMOS analog integrated circuits, gain control, optical wireless links.**

I. INTRODUCTION

THE most critical building block for optical wireless system performance in terms of speed and sensitivity is the optical receiver front-end circuit. Complementary metal-oxide-semiconductor (CMOS) technologies have emerged as the most cost-effective alternative for high-performance optical communication circuits offering superior integration capabilities and low-power operation compared to power-hungry III-V processes (GaAs, InP-based HEMT); and high transition frequencies ($f_T \sim 250GHz$) due to decades of aggressive gate-length scaling (<45nm).

For free-space communication, the TIA design optimization mandates additional challenges unknown to fiber-optic receivers. The input capacitance, including the detector depletion capacitance and packaging parasitics at the opto-electronic interface, is a key parameter for optical receiver design evaluation. For efficient fiber-to-detector coupling, the detector capacitance considered in TIA designs are as low as 150fF to 1pF [1]–[3]. To fully realize the bandwidth capabilities of optical wireless links, line-of-sight (LOS) channels are the optimal approach. However, to achieve high optical gain and wide-FOV at the receiver requires a large detector area with associated capacitance which makes it difficult to achieve high-speed performance at low-power. Furthermore, a wide receiver dynamic range is required to accommodate link distance and angle variation while maintaining a stable response.

Optical wireless system operation in the O-band (1.3μm) and C-band (1.5μm) is preferred as eye safety requirements allow 20 times higher transmit power levels compared to the 850nm band [4]. To achieve optimal transceiver performance requires hybrid integrated components combining the superior optical properties of III/V materials with high-speed mixed-signal CMOS circuits in unmodified processes [5]. Such hybrid components introduce deleterious parasitic capacitance at the input node which degrades receiver sensitivity and limits the maximum achievable bandwidth. For fully integrated optical wireless receivers, a front-end TIA architecture with insensitivity to input capacitance is required.

To minimize the sensitivity to input parasitic capacitance at the receiver front-end, several CMOS circuit techniques have been reported, including common-gate input topologies [6], [7], regulated cascode configurations [8], and bootstrapping techniques [9]. A major drawback of the common-gate topology for optical wireless detectors is the large common-gate transconductance required to isolate the input capacitance results in large junction capacitances that offset any performance improvement. In addition, the input stage biasing network introduces

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additional noise at the input, thus reducing sensitivity. Bootstrapping typically requires a higher supply voltage for the bootstrap follower and the photodiode.

To accommodate varying link distances and transmitter-receiver angle orientation in optical wireless systems, a variable gain front-end TIA is required at the receiver to widen the dynamic range. A TIA feedback amplifier topology employing a tunable feedback resistance [10]–[12] is widely used to widen dynamic range. However, this configuration is difficult to stabilize. The use of pass transistor arrays [12] to realize variable resistors for gain tuning can introduce a bandwidth penalty and greater sensitivity to process variations. Current-mode gain control schemes have been implemented employing current switches and attenuators at the input to steer high photocurrent signals away from the TIA input [13], [14]. Such techniques require bipolar input stages and introduce additional challenges in biasing the detector at the input node.

The presented work exploits a CMOS capacitive-feedback TIA (CF-TIA) topology with several improvements over the basic design reported in [15] to achieve performance requirements for fully integrated optical wireless transceivers. A self-biased automatic gain control (AGC) implemented within the capacitive feedback configuration provides a more stable frequency performance as the transimpedance gain is tuned. Furthermore, a DC level correction circuit is employed to enable DC coupling to subsequent stages. Section II analyzes the optical wireless receiver sensitivity budget which provides a design guideline for receiver noise. Section III presents a qualitative comparison between resistive-feedback and capacitive-feedback TIA structures followed by a discussion of the core TIA design and AGC circuits. Section IV describes the experimental results, including electrical and optical measurements. Finally, conclusions are drawn in Section V.

II. Optical Wireless Receiver Sensitivity Budget

To enable CMOS circuit design optimization in terms of area, power, gain, and bandwidth, it is important to determine the noise requirement based on the required sensitivity for a particular target bit error rate (BER) and link range.

The optical receiver sensitivity is defined in terms of the minimum average optical power, P_{min}^{opt} , required to achieve a particular bit error rate (BER), according to the following expression:

$$BER = Q\left(\frac{P_{min}^{opt} \cdot R_{ph}}{I_{n,RMS}}\right) \tag{1}$$

where $Q(\cdot)$ is the Q function and can be approximated with high accuracy by:

$$Q(x) \approx \frac{1}{x\sqrt{(2\pi)}} exp\left(-\frac{x^2}{2}\right), x > 3 \tag{2}$$

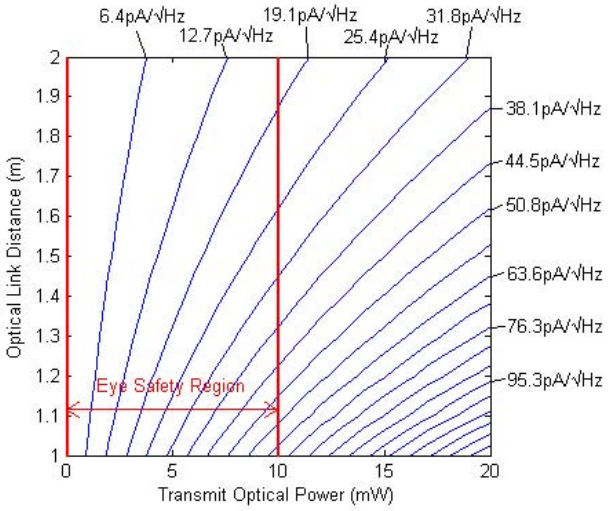

Fig. 1. Input-referred current noise budget.

and R_{ph} is the detector responsivity in A/W. The square-root of the input-referred noise-current spectral density integrated over the receiver's noise equivalent bandwidth (NEB), Δf, yields the total mean-square input-referred noise current, $I_{n,RMS}$.

$$I_{n,RMS} = \sqrt{\overline{I_n^2} \cdot \Delta f} \tag{3}$$

$I_{n,RMS}$ in Equation 1 can also be expressed in terms of the signal-to-noise ratio (SNR) as:

$$BER = Q\left(\frac{SNR}{2}\right) \tag{4}$$

From Equations 2 and 4 the required SNR for a BER of 10^{-12} is 14 for random nonreturn-to-zero (NRZ) data in the presence of Gaussian noise. From 1, 3 and 4, the maximum tolerable input-referred noise-current spectral density in terms of the sensitivity is:

$$\overline{I_n^2} = \left(\frac{2 \cdot P_{min}^{opt} \cdot R_{ph}}{SNR}\right)^2 / \Delta f \tag{5}$$

To estimate the receiver noise requirement, we consider power losses in short-distance optical wireless links due to free-space transmission and opto-electrical energy conversion. The transmitter is modeled as a Lambertian optical emitter. The received optical power can be estimated from the optical link model as follows [16]:

$$P_{rx}^{opt} = \frac{n+1}{2\pi} \cdot \frac{P_{tx}^{opt}}{r^2} \cdot A \cdot \cos^n \varphi \cdot \cos\theta \tag{6}$$

where P_{tx}^{opt} is the transmitted optical power, r is the distance between the transmitter and the receiver, A is the effective collecting area of the receiver, φ is the angle of emission, θ is the angle of incidence, and

$$n = \frac{-\ln(2)}{\ln(\cos(\Phi_{1/2}))} \tag{7}$$

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where $\Phi_{1/2}$ is the half-power semi-angle. For short-distance optical wireless link applications, assume $A = 5mm^2$, $R_{ph} = 0.9A/W$, and $\Phi_{1/2} = 30^\circ$ from previous work. We consider the simplest case where the receiver is placed co-axis with the transmitter ($\varphi = \theta = 0$). Based on Equations 5-7, Figure 1 plots a numerical estimation of the maximum tolerable input-referred noise contour curves in terms of transmit optical power and optical link distance, for a target BER of 10^{-12} and with a TIA -3dB bandwidth of 500MHz. The transmit optical power level is 10mW, which is the maximum allowed power for Class 1 eye safe operation at 1550nm. Within the eye safety range, if the target optical link distance is 1.5m, then the maximum tolerable input-referred noise can be read from Figure 1 as approximately $30pA/\sqrt{(Hz)}$. This can be defined as an upper design limit for the allowed photodiode and amplifier noise as:

$$\overline{I_n^2} = \overline{I_{PD}^2} + \overline{I_{n,TIA}^2} \tag{8}$$

The predominant detector noise source is shot noise with noise power spectral density given by:

$$\overline{I_{PD}^2} = 2qI_D \tag{9}$$

where q is the electron charge, and I_D is the average photodiode current. Based on assumptions stated above, the received optical power is around -20dBm, which corresponds to a RMS shot-noise current spectral density due to the detector that is much smaller than the upper design limit of $30pA/\sqrt{(Hz)}$. Thus, the RMS input-referred noise spectral density limit for the transimpedance amplifier circuit can be approximately set at $30pA/\sqrt{Hz}$.

III. Circuit Architecture

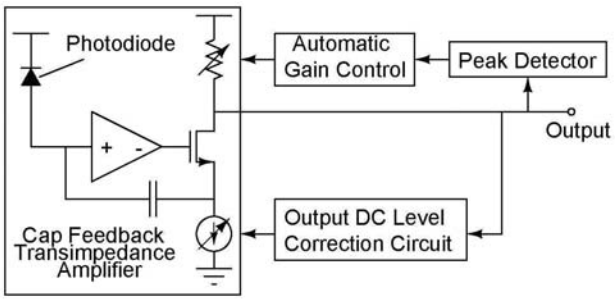

Fig. 2. Front-end transimpedance amplifier architecture.

The receiver front-end architecture is shown in Figure 2. The core TIA implements a capacitive-feedback configuration to decouple the variable transimpedance gain element from the feedback path to minimize impact on bandwidth and stability. An automatic gain control (AGC) circuit is implemented to adjust the variable gain by monitoring the output voltage swing. This variable gain configuration improves the input current swing that the TIA can accept, thus making it more practical for use in line-of-sight (LOS) optical wireless applications. Another output DC level correction circuit is implemented to set a constant output DC level for the DC coupling of the TIA to the post-amplifier circuit.

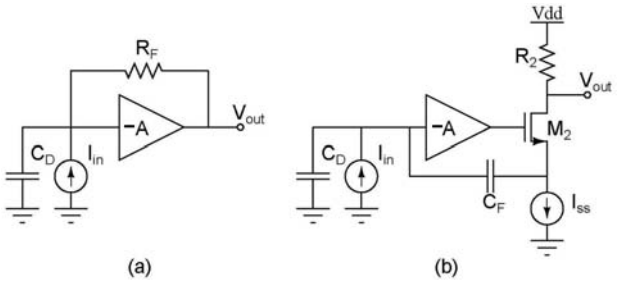

Fig. 3. (a) Traditional resistive-feedback TIA topology, (b) capacitive-feedback TIA topology.

A. Resistive-feedback TIA vs. Capacitive-feedback TIA

For the common resistive-feedback TIA topology shown in Figure 3(a), the gain and bandwidth are expressed as:

$$Z_T(0) = \frac{A}{A+1}R_F \tag{10}$$

$$w_{-3dB} = \frac{A+1}{R_F C_D} \tag{11}$$

The capacitance C_D represents the input parasitic capacitance including contributions from the large photodiode, electrostatic discharge (ESD) protection diode, and input bondpad/package lead. As the feedback resistance is tuned, there is a direct trade-off between bandwidth, closed-loop stability, and gain. In addition, as the feedback resistance is reduced, its noise contribution increases and degrades receiver sensitivity.

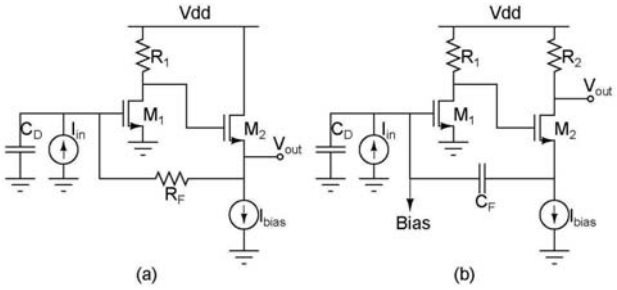

Fig. 4. Transistor-level schematic: (a) traditional resistive-feedback TIA circuit, and (b) capacitive-feedback TIA circuit.

The TIA reported here exploits a capacitive-feedback approach, where A is the core voltage amplifier gain, and the feedback element C_F=2pF returns a current from the source node of M_2. The output is taken from the drain of M_2, this feedback connection prevents loading on the output node.

A transistor level schematic of the capacitive-feedback TIA topology is shown in Figure 4(b). This design yields a bandpass response with an upper cut-off frequency and transimpedance midband gain given by:

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$$Z_T = \frac{R_2 \cdot C_F(1+A)}{C_F(1+A)+C_D} \tag{12}$$

$$w_{-3dB} \approx \frac{(1+A)\cdot g_{m2}}{C_X} \tag{13}$$

where C_X denotes the equivalent series capacitance of C_D and the miller capacitance of C_F as given by:

$$C_X = \frac{1}{\frac{1}{C_D} + \frac{1}{(1+A)\cdot C_F}} \tag{14}$$

The amplifier routes the input photocurrent signal to the drain of M_2 and amplifies it by R_2. The bandwidth expression in Equation (13) reveals that the bandwidth is primarily a function of the the transconductance g_{m2} and C_X, while being insensitive to R_2 tuning. This is achieved by splitting the output node and the feedback node, which corresponds to the drain and source of M_2, respectively. Furthermore, the equivalent input capacitance, C_X, is smaller than either C_D or $(1+A)C_F$, thus minimizing sensitivity to photodiode capacitance.

For a qualitative comparison of frequency response, both topologies are implemented with a two-pole open-loop response with equivalent open-loop mid-band gain A. The bias network for Figure 4(b) can be found in Figure . Figure 5 plots the simulated frequency response as function of variation in the photodiode capacitance from 0.25pF to 5pF for the two configurations. The transimpedance bandwidth remains within 20% over the detector capacitance variation of 0.25pF to 5pF compared to 90% degradation for the traditional resistive feedback topology. Figure 6 compares the impact of gain tuning on the transimpedance bandwidth. For accurate comparison, the detector capacitance for both topologies is chosen to achieve equal bandwidth at maximum gain. Insensitivity to gain tuning is shown as an additional advantage of the capacitive feedback topology; the bandwidth remains within 50% variation over a 24dB variation in transimpedance gain. As shown in Figure 6, for the resistive-feedback TIA circuit there is a large increase in bandwidth as the gain decreases which results in circuit instability.

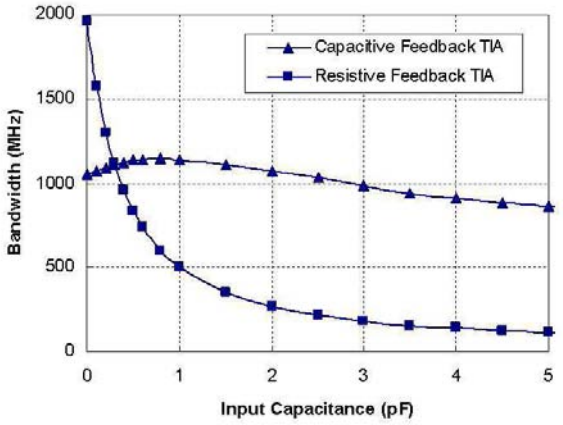

Fig. 5. Transimpedance bandwidth as a function of photodiode capacitance for different TIA configurations.

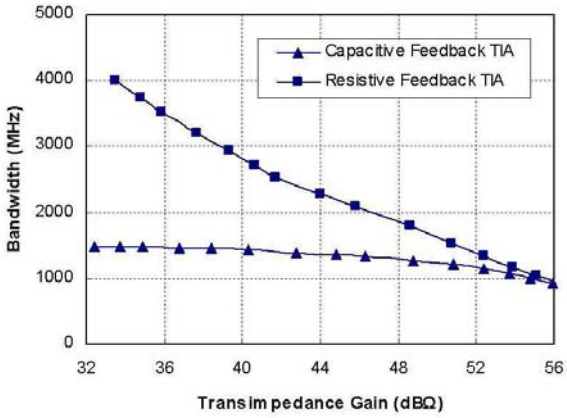

Fig. 6. Transimpedance bandwidth as a function of gain for different TIA configurations.

B. Noise Analysis

The noise expression for the resistive feedback topology in Figure 4(a) can be expressed as:

$$\begin{aligned}\overline{i_{n,EQ}^2} \cong\ & \frac{4kT}{R_F} + \left[\frac{4kT}{R_1}\frac{1}{g_{m1}^2} + \frac{4kT\gamma}{g_{m1}}\right] \\ & \times \left(\frac{1}{R_F^2} + (2\pi f)^2 (C_D)^2\right) \\ & + \frac{4kT\gamma}{g_{m2}}\frac{1}{A^2}\cdot\left(\frac{1}{R_F^2} + (2\pi f)^2(C_D)^2\right)\end{aligned} \tag{15}$$

where k is the Boltzman constant, T is the absolute temperature, γ is the noise factor of the MOSFET device. The first term in (15) is the noise contributed by the feedback resistor R_F. The second term represents the noise contributed by the core voltage amplifier which consists of M_1 and R_1. The third term is the noise of transistor M_2 in the output stage. The noise expression for the capacitive feedback topology is derived in Appendix A and given by:

$$\begin{aligned}\overline{i_{n,EQ}^2} \approx\ & \frac{4kT}{R_2}\cdot\left(1 + \frac{(2\pi f)^2 (C_X)^2}{g_{m2}^2}\right) \\ & + \left[\frac{4kT}{R_1}\frac{1}{g_{m1}^2} + \frac{4kT\gamma}{g_{m1}}\right]\cdot(2\pi f)^2(C_X)^2 \\ & + \frac{4kT\gamma}{g_{m2}}\frac{1}{A^2}\cdot(2\pi f)^2(C_X)^2\end{aligned} \tag{16}$$

The first term in (16) is the noise contributed by the load resistor R_2. Similar to resistive-feedback TIA noise expression, the second term represents the noise contributed by the core voltage amplifier which consists of M_1 and R_1. The third term is the noise contribution of transistor M_2 in the output stage.

At low frequencies, the noise contribution of the gain element R_F in the resistive-feedback TIA and R_2 in the

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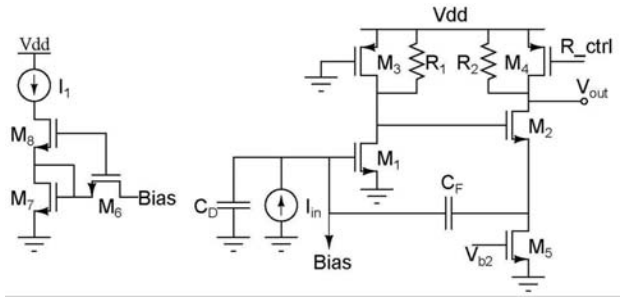

Fig. 7. Capacitive-feedback TIA implementation.

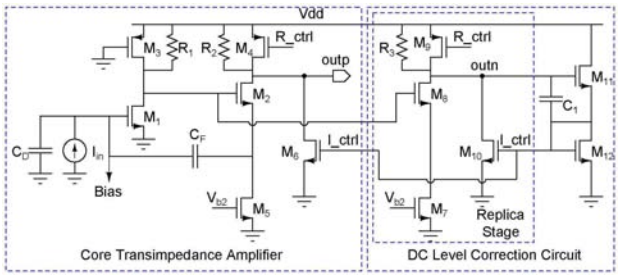

Fig. 8. Core TIA with output DC level correction.

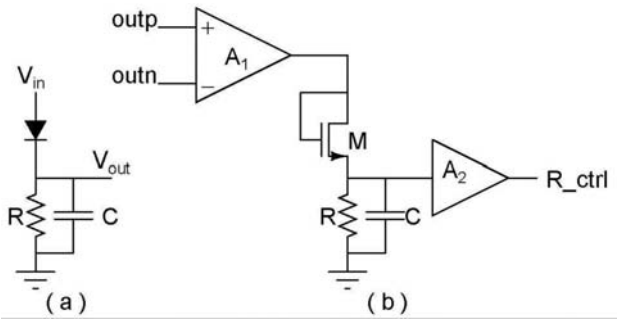

Fig. 9. Peak voltage detector configuration.

capacitive-feedback TIA are dominant. At high frequencies, the thermal noise contribution of M_1 is dominant for both topologies. Comparing the second term in (15) and (16), it is seen that the capacitive-feedback topology achieves better noise performance due to the equivalent capacitance C_X, given in (14), being smaller the photodiode capacitance C_D.

C. Transimpedance Amplifier Design

Figure 7 illustrates the implementation of the core amplifier and input bias circuit. To maximize the core voltage amplifier open-loop gain A, R_1 is placed in parallel with a PMOS current source to allow a larger R_1 and higher M_1 transconductance without suffering from a large voltage drop. The bias current for the output stage is supplied by M_5. The gain element is defined by a triode-mode PMOS in parallel with R_2, which provides a more linear overall resistance with tuning. For the bias network, M_1 and M_7 constitute a current mirror, I_1 and M_8 define the on-resistance of M_6, which provides a large resistance to isolate the signal path from the low impedance introduced by M_7.

The variable resistor realized by M_4 works in linear-mode. The resistance of the PMOS transistor in linear mode is calculated as:

$$R = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{sg} - |V_{th,p}|)} \tag{17}$$

The size of the transistor and its gate voltage were chosen in order to achieve the desired resistance range from 700Ω to 200Ω with gate voltage varying from 1.8V to 0V.

An undesirable feature of implementing AGC by varying the load resistance at the output node is the shift in DC output voltage, preventing direct coupling to the next stage. To enable DC coupling of the TIA to following stages, the AGC is designed to set the DC output node level as the gain element is varied. As illustrated in Figure 8, an output DC level correction circuit is implemented to set the output voltage level to a nearly constant value.

In order to avoid loading of the DC correction circuit at the output node, M_7, M_8, M_9 and M_{10} constitute a replica of the TIA output stage, with the same input from the core voltage amplifier stage. M_{11} and M_{12} sense the output level of the replica stage. As the TIA load resistance varies, M_{11}, M_{12}, M_6 and M_{10} operate as a negative feedback network to compensate the DC output voltage change by adjusting current sources M_6 and M_{10}. Here, the DC correction control voltage is applied to current sources M_6 and M_{10} (rather than M_5 and M_7) to prevent changing the current flow through M2, and thus avoid altering the small signal characteristics of the output stages. A capacitor C_1 is connected between the replica output node and the gates of the current sources. It provides a low frequency cut off corner to ensure the DC correction circuit only processes the output DC component without impacting the small-signal behavior of the circuit.

D. Automatic Gain Control Design

With the photodetector biased such that the photocurrent signal is driven into the amplifier, the TIA output stage is driven out of saturation for large input current amplitudes, resulting in signal distortion. To mitigate this effect, the gain element is dynamically adjusted by tuning its gate voltage as the input current increases. For input current levels below the AGC threshold, the TIA gain is held at maximum. A peak detector is implemented at the output of the transimpedance amplifier to sense the amplitude of the output swing which is proportional to the amplitude of the received optical power. Figure 9(a) is a simple schematic of the peak detector consisting of a diode and RC network. However, detecting signals with very small amplitudes is inaccurate and even worse at high frequencies. To boost the peak detector input signal, a differential preamplifier A_1 is implemented; and to boost the gate control voltage for the variable gain element, a post-amplifier A_2 is added after the peak detector, as shown in Figure 9(b). The two inputs of the

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differential amplifier are supplied from the output node 'outp' and the corresponding node 'outn' of the replica stage (see Figure 8). Since node 'outn' tracks the DC level of node 'outp', only the AC swing of the output signal will be amplified. The circuit implementation of the peak detector block is shown in Figure 10.

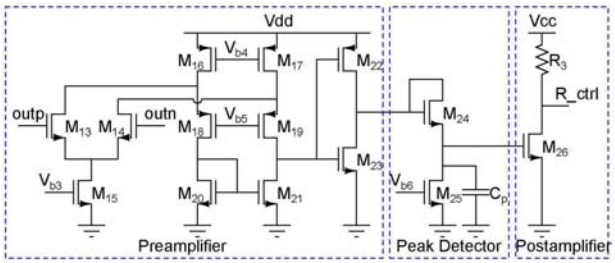

Fig. 10. AGC implementation.

Amplifier A_1 is implemented with a folded differential amplifier followed by an inverting amplifier. Device M_{24} is a diode connected NMOS transistor. The discharging resistor in Figure 9 is realized by M_{25}, which operates in the deep triode region. The post-amplifier is a simple common-source amplifier. For accurate gate control of M_4 and M_9 ranging from 0V to 1.8V, a separate 1.8V power supply is utilized for the post-amplifier circuit A_2 to guarantee the two rail voltages are exactly 0V and 1.8V. Thus, when the input current is smaller than the threshold of the AGC control region, R_{ctrl} will remain steady at 1.8V and the gain will yield the maximum value.

Figure 11 shows the simulated output voltage amplitude of the TIA and the transimpedance gain provided by the TIA with automatic gain control. The transimpedance gain varies from 52dBΩ to 36dBΩ with input current peak-peak varying from 10μA to 1.2mA. It can be seen from the plot that the maximum gain is sustained up to input current amplitudes of 100μA, and subsequent increasing in input signal results in a decrease in transimpedance gain.

IV. Experimental Results

Test chips of the capacitive-feedback TIA were implemented in a low-cost 0.5μm CMOS technology. Figure 12 shows the microphotograph of the core chip with an area of 210μm×280μm without pads. For electrical characterization, a photodetector emulation circuit, as show in Figure 13, is used consisting of a voltage source (pulse pattern generator) in series with a large variable resistor (10kΩ) to model the photocurrent signal. The large series resistor prevents the signal source from lowering the TIA input impedance. A variable off-chip capacitor is used to model the photodiode capacitance at the input of the transimpedance amplifier for frequency response measurement.

Figure 14 shows the measured frequency response compared with simulation results. For a total input capacitance of C_D=0.5pF (including trace, package and bondpad parasitics), the measured transimpedance gain is 55dBΩ

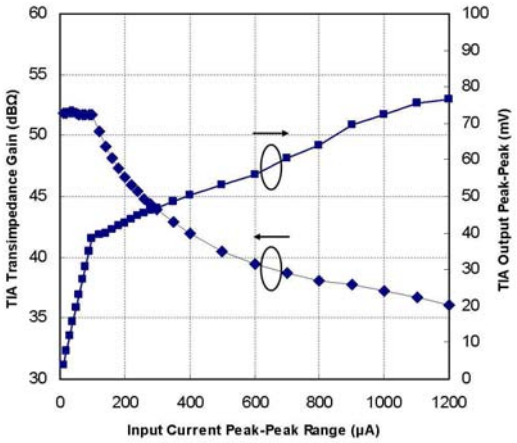

Fig. 11. TIA transimpedance gain and TIA output voltage swing within the input current dynamic range.

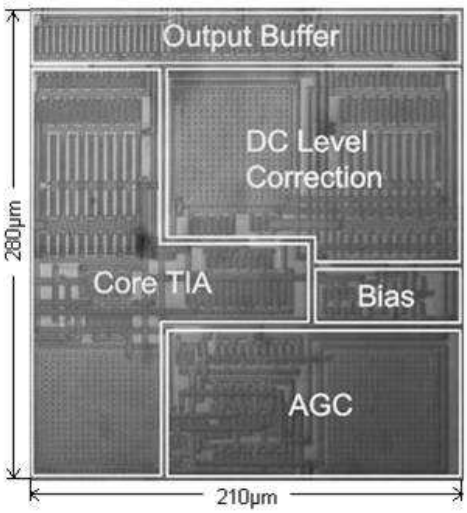

Fig. 12. Chip microphotograph of the transimpedance amplifier.

and the -3dB bandwidth is 532MHz. With C_D=5pF, the transimpedance gain is 52dBΩ and the -3dB bandwidth is 523MHz. Thus, as the input capacitance increases by an order of magnitude from 0.5pF to 5pF, the -3dB bandwidth remains within 5%. This demonstrates the key merit of capacitive feedback structure over conventional resistive feedback structure, of which the -3dB bandwidth will decrease nearly proportional to the increase of input capacitance. The circuit exhibits a bandpass response with a lower cut-off frequency set to 100kHz.

Figure 15 illustrates the measured eye diagrams at 750Mbits and 1Gbits respectively, with 5pF input capacitance. The 50μA peak-peak input current is patterned by a Manchester-coded data sequence, which reduces clock/data recovery complexity. The data sequence was coded from a 2^{14}-1 pseudorandom binary sequence (PRBS).

In order to characterize the automatic gain control (AGC) and output DC correction feature of the TIA,

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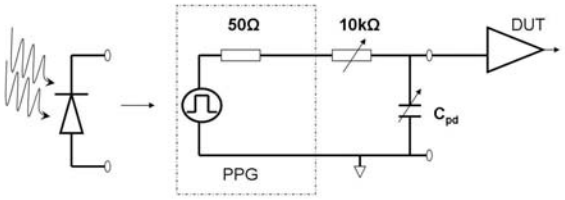

Fig. 13. Photodetector emulation circuit for electrical characterization.

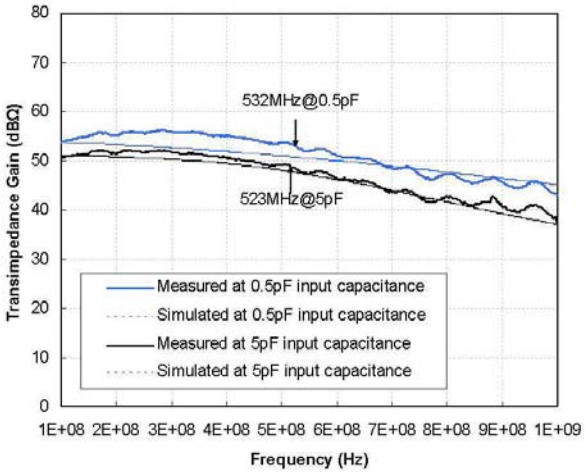

Fig. 14. Measured and simulated frequency response.

two I/O pads were connected to probe the variable gain control voltage and DC correction control voltage, which correspond to node R_ctrl and node I_ctrl, respectively in Figure 8. The measured R_ctrl and I_ctrl voltage levels at various input current amplitudes from 10μA to 1.2mA are shown in Figure 16. The input current is varied by setting the voltage signal source amplitude and series resistor.

For noise measurements, an external amplifier is mounted on the PCB at the output of the CMOS TIA chip to raise the output noise level above the noise floor of the spectrum analyzer (Agilent E4408B). Figure 17 presents the simulated and measured equivalent input-referred noise current spectral density taking into account the transimpedance gain and the external amplifier gain. The input-referred noise current is 22pA/$\sqrt{Hz}$ at 523MHz for an input photodetector capacitance of 5pF. The total input-referred noise current spectral density is integrated over the 523MHz bandwidth. To achieve a bit error rate of 10^{-12}, the minimum TIA input current amplitude is 8.8μA.

For optical measurements of the transimpedance amplifier, the optical test setup is shown in Figure 19. A 1550nm continuous wave light source (Thorlabs SIFC1550) is externally modulated by a 10Gbit/s electro-absorption modulator (CIP 10G-LR-EAM-1550). The Anritsu MP1800A pulse pattern generator provides a high-speed data sequence to drive the modulator. An InGaAs

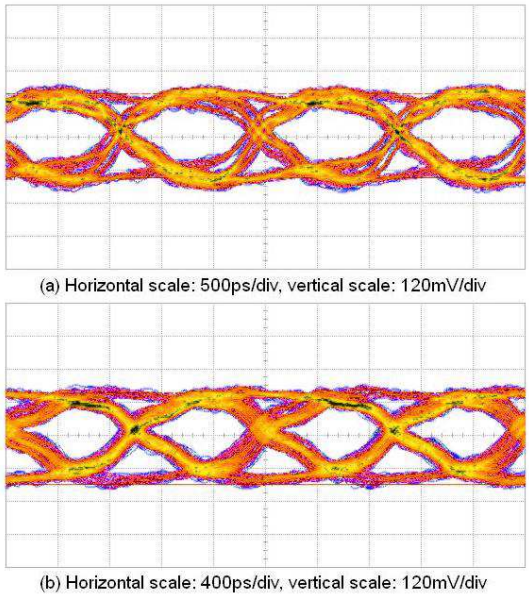

Fig. 15. Measured eye diagram at (a) 750 Mb/s and (b) 1Gb/s using a 2^{14}-1 pseudorandom, manchester-coded bit sequence with 50μA photocurrent.

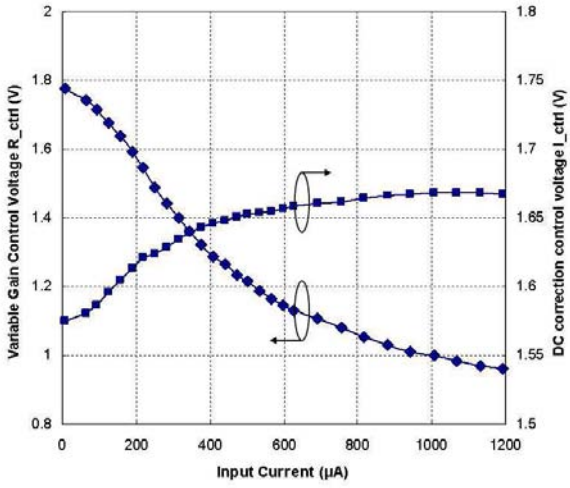

Fig. 16. Variable gain control voltage (R_ctrl) and DC correction control voltage (I_ctrl) versus input current.

photodiode (Thorlabs FGA04) is mounted on an FR-4 printed circuit board (PCB) at the input of the CMOS TIA chip. The photodiode has a bandwidth of 2GHz and its responsivity is 0.9A/W at a wavelength of 1550nm; the parasitic capacitance is approximately 1pF at a reverse bias voltage of 2V.

Figure 18 illustrates the measured eye diagrams at 750Mbit/s with input optical power of 0dBm. Further eye diagram measurement at the minimum and maximum optical power levels are limited by the available equipment. The incident light was modulated by RF signal with a Manchester-coded data sequence. The Manchester data sequence was coded from a 2^{14}-1 pseudorandom binary sequence (PRBS).

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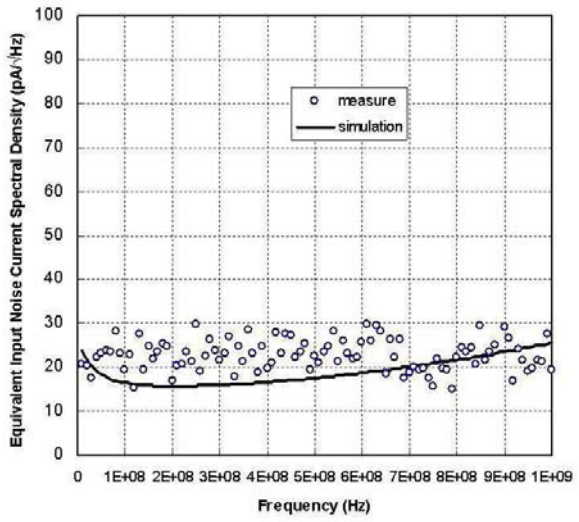

Fig. 17. Simulated and measured equivalent input-referred noise current spectral density.

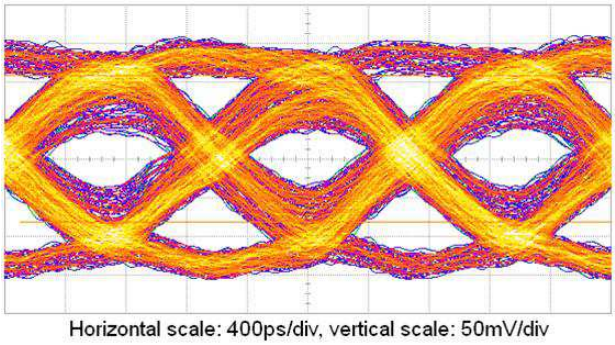

Fig. 18. Measured eye diagram at -17dBm receiver input optical power at 750Mb/s.

A comparison of the presented work alongside recently reported CMOS optical receiver front-ends for integration with large area, wide FOV detectors in optical wireless links is given in Table I. In [12] and [17], the transimpedance bandwidth is inversely proportional to the photodiode capacitance, resulting in a significant change in bandwidth as the input capacitance varies. For gain control, the TIA reported in [12] implements variable resistors realized by a digitally-controlled pass transistor array. However, the gain is controlled at discrete levels and the pass transistors introduce a speed penalty, as well as, susceptibility to process variations. The current-mode TIA presented in [18] does not report the bandwidth expression, and thus it is difficult to determine the bandwidth, gain, and input capacitance dependence. This work achieves a higher bandwidth with greater insensitivity to transimpedance gain and input capacitance up to 5pF.

V. Conclusion

An integrated front-end transimpedance amplifier with capacitive feedback configuration has been presented for use in broadband optical wireless links operating at 750Mbit/s. This transimpedance amplifier implements an automatic gain control circuit and achieves a dynamic gain range from 52dBΩ to 36dBΩ. The -3dB bandwidth is 523MHz for 5pF input capacitance and 532MHz for 0.5pF input capacitance. It achieves an input-referred current noise of 22pA/$\sqrt{Hz}$ for 5pF input capacitance. The chip area is 0.06mm^2 not including pads. The power dissipation is 53mW.

TABLE I
Performance Comparison of Recent CMOS TIAs for Optical Wireless Communication

	[12]	[17]	[18](sim.)	**This work**
Technology	0.35μm	0.7μm	0.35μm	0.5μm
C_{in}	5pF	6-10pF	5pF	0.5-5pF
Bandwidth	70MHz	155MHz	114MHz	532-523MHz
Transimpedance Gain	85-54dBΩ	72dBΩ	60dBΩ	52-36dBΩ
$f_{-3dB} \propto \frac{1}{C_{pd}}$	Yes	Yes	Unknown	No
Gain Control	Discrete Levels	No	No	Self-Biased, Continuous

Appendix A
Noise Analysis of the Capacitive-Feedback TIA

Figure 20 shows the noise-perturbed circuit schematic of the capacitive-feedback TIA, which ignores the output stage bias current source. In this analysis, shot noise and flicker noise are ignored. A small-signal analysis yields the following equations of the summed currents at the input node and source/drain of transistor M_2:

$$V_{g1} \cdot sC_D - I_{in} = (V_{s2} - V_{g1}) \cdot sC_F \tag{A.1}$$

$$(-V_{g1} g_{m1} R_1 - V_{s2}) g_{m2} = V_{g1} \cdot sC_D - I_{in} \tag{A.2}$$

$$(V_{s2} - V_{g1}) \cdot sC_F = \frac{V_{out}}{R_2} \tag{A.3}$$

where V_{g1} is the gate voltage of M1 and V_{s2} is the source voltage of M_2. For optical wireless applications, the large input photodetector capacitance C_D dominates over the gate capacitance of M_1 and M_2. Thus, the analysis only considers C_D. From Equations (A.1) - (A.3), the transimpedance gain V_{out}/I_{in} can be expressed as:

$$\begin{aligned} \frac{V_{out}}{I_{in}} &= \frac{g_{m2} R_2 [C_F(1 + g_{m1} R_1) + C_D]}{g_{m2}[C_F(1 + g_{m1} R_1) + C_D] + sC_F C_D} \\ &\approx \frac{g_{m2}[g_{m1} R_1 C_F + C_D]}{g_{m2}[g_{m1} R_1 C_F + C_D] + sC_F C_D} \cdot R_2 \end{aligned} \tag{A.4}$$

First, the output noise voltages due to the channel thermal noise of M_1 and M_2 are given by (A.5) and (A.6), respectively, assuming $g_{m1} R_1 \gg 1$. The output noise voltages due to the thermal noise of R_1 and R_2 are given by (A.7) and (A.8), respectively.

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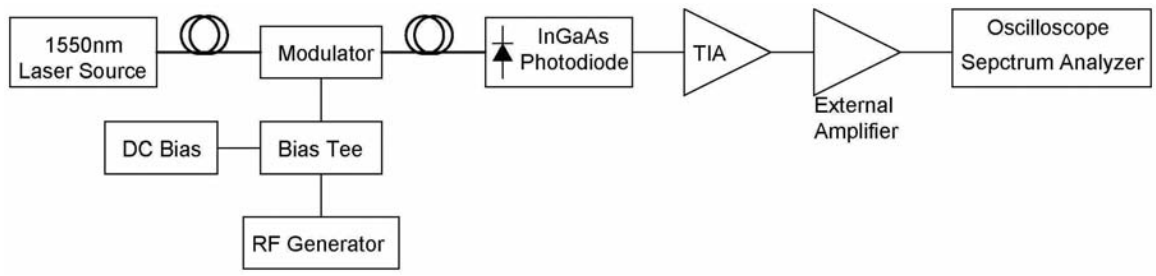

Fig. 19. Optical setup.

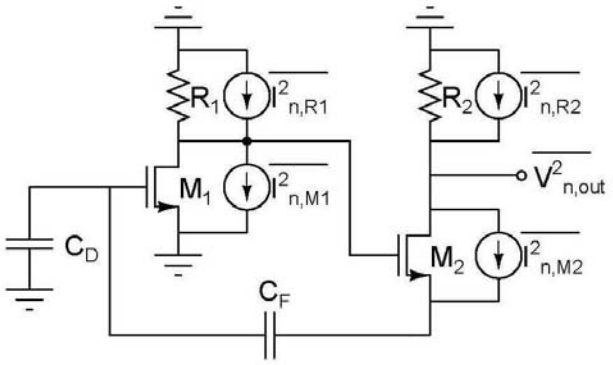

Fig. 20. Noise-perturbed circuit of the capacitive-feedback TIA.

$$V_{o1} \approx \frac{sR_1R_2g_{m2}C_FC_D}{g_{m2}[g_{m1}R_1C_F + C_D] + sC_FC_D} \cdot \overline{I_{n,M1}} \quad \text{(A.5)}$$

$$V_{o2} \approx \frac{sR_2C_FC_D}{g_{m2}[g_{m1}R_1C_F + C_D] + sC_FC_D} \cdot \overline{I_{n,M2}} \quad \text{(A.6)}$$

$$V_{o3} \approx \frac{sR_1R_2g_{m2}C_FC_D}{g_{m2}[g_{m1}R_1C_F + C_D] + sC_FC_D} \cdot \overline{I_{n,R1}} \quad \text{(A.7)}$$

$$V_{o4} \approx R_2 \cdot \overline{I_{n,R2}} \quad \text{(A.8)}$$

Finally, the output noise voltage V_{o5} due to the equivalent input noise current source $\overline{I_{n,EQ}}$ can be expressed as:

$$V_{o5} \approx \frac{g_{m2}R_2(g_{m1}R_1C_F + C_D)}{g_{m2}[g_{m1}R_1C_F + C_D] + sC_FC_D} \cdot \overline{I_{n,EQ}} \quad \text{(A.9)}$$

By equating (A.9) to the sum of noise voltages in (A.5) - (A.8), the equivalent input noise current spectral density is given by:

$$\begin{aligned}\overline{i^2_{n,EQ}} \approx\ & \frac{4kT}{R_2} \cdot \left(1 + \frac{(2\pi f)^2(C_X)^2}{g^2_{m2}}\right) \\ & + \left[\frac{4kT}{R_1}\frac{1}{g^2_{m1}} + \frac{4kT\gamma}{g_{m1}}\right] \cdot (2\pi f)^2(C_X)^2 \\ & + \frac{4kT\gamma}{g_{m2}}\frac{1}{A^2} \cdot (2\pi f)^2(C_X)^2 \quad \text{(A.10)}\end{aligned}$$

where A=$g_{m1}R_1$ is the mid-band gain of the core amplifier, and C_X denotes the equivalent series capacitance of C_D and the miller capacitance of C_F.

$$C_X = \frac{1}{\frac{1}{C_D} + \frac{1}{AC_F}} \quad \text{(A.11)}$$

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REFERENCES

[1] A. Schild, H.-M. Rein, J. Mullrich, L. Altenhain, J. Blank, and K. Schrodinger, "High-gain sige transimpedance amplifier array for a 12 x 10 gb/s parallel optical fiber link," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 4–12, Jan. 2003.

[2] J. Baek, J. Kwon, J. Park, D. Rhee, E. Lee, J. Lee, Y. Oh, and D. Jang, "Low-cost and high-performance apd burst-mode receiver employing commercial tia for 1.25-gb/s epon," *IEEE Photonics Tech. Letters*, vol. 17, no. 10, pp. 2170–72, Oct. 2005.

[3] W.-Z. Chen and C.-H. Lu, "Design and analysis of a 2.5-gbps optical receiver front-end in a 0.35-um digital cmos technology," *IEEE Trans. Circ. and Systems I*, vol. 53, no. 4, pp. 977–83, Apr. 2006.

[4] "Ansi $z136.1$ american national standard for safe use of lasers ($http : //www.laserinstitute.org/store/ansi/106ae$)." 2007.

[5] D. O'Brien, G. Faulkner, K. Jim, E. Zyambo, D. Edwards, M. Whitehead, P. Stavrinou, G. Parry, J. Bellon, M. Sibley, V. Lalithambika, V. Joyner, R. Samsudin, R. Atkinson, D. Holburn, and R. Mears, "Integrated transceivers for optical wireless communications," *IEEE J. Sel. Topics in Quantum Electron.*, vol. 11, no. 1, pp. 173–83, Jan/Feb 2001.

[6] C. Toumazou and S. Park, "Wideband low noise cmos transimpedance amplifier for gigahertz operation," *Electron. Lett.*, vol. 32, no. 13, pp. 1194–96, June 1996.

[7] S. Mohan, M. Henderson, S. Boyd, and T. Lee, "Bandwidth extension in cmos with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, March 2000.

[8] S. Park and C. Toumazou, "A packaged low-noise high-speed regulated cascode transimpedance amplifier using a 0.6μm n-well cmos technology," *in Proc. European Solid-State Circuits Conf.*, pp. 431–434, Sept. 2000.

[9] C. Hoyle and A. Peyton, "Shunt bootstrapping technique to improve bandwidth of transimpedance amplifiers," *Electronics Letters*, vol. 35, no. 5, pp. 369–70, March 1999.

[10] Q. Le, S.-G. Lee, Y.-H. Oh, H.-Y. Kang, and T.-H. Yoo, "A burst-mode receiver for 1.25-gb/s ethernet pon with agc and internally created reset signal," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 2379–88, Dec. 2004.

[11] W.-Z. Chen, Y.-L. Cheng, and D. Lin, "A 1.8-v 10-gb/s fully integrated cmos optical receiver analog front-end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1388–96, June 2005.

[12] K. Phang and D. A. Johns, "A CMOS optical preamplifier for wireless infrared communications," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 7, pp. 852–859, July 1999.

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[13] T. Ruotsalainen, P. Palojärvi, and J. Kostamovaara, "A wide dynamic range receiver channel for a pulsed time-of-flight laser radar," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1228–38, Aug. 2001.

[14] L. van den Broeke and A. Nieuwkerk, "Wide-band integrated optical receiver with improved dynamic range using a current switch at the input," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 862–4, July 1993.

[15] B. Razavi, "A 622Mb/s 4.5pa/$\sqrt{Hz}$ CMOS transimpedance amplifier," *IEEE International Solid-State Circuits Conference*, pp. 162–163, Feb. 2000.

[16] K. Sterckx, J. Elmirghani, and R. Cryan, "Three-segment pyramidal fly-eye detection antenna for optical wireless communication systems under the constraints of ambient noise introduced by highly directive spot lights," *Int. J. of Commun. Sys.*, vol. 13, pp. 577–88, 2000.

[17] V. Joyner, D. Holburn, D. O'Brien, and G. Faulkner, "A cmos imaging diversity receiver chip with flip-chip integrated detector array for optical wireless links," *Proc. IEEE Laser and Electro-Optics Society Annual Meeting*, pp. 927–928, Nov. 2006.

[18] R. Chen, T.-S. Hung, and C.-Y. Hung, "A CMOS infrared wireless optical receiver front-end with a variable-gain fully differential transimpedance amplifier," *IEEE Trans. on Consumer Electronics*, vol. 51, no. 2, pp. 424–429, May 2005.

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