Design and Implementation of Communication Digital FIR Filter for Audio Signals on the FPGA Platform

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***Abstract*—Digital Signal Processing (DSP) in telecommunications is widely used for its outstanding performance. Hence, optimal results would be obtained with the sophisticated design and implementation of the digital Finite Impulse Response (FIR) filter. In this paper, the design and implementation of the FIR filter for processing the audio signal are obtained through the Field-Programmable Gate Array (FPGA) platform -Altera DE1 board. The design is divided into three primary blocks, which are the S2P Adapter block, Codec initialization block, as well as FIR filter block, which were then interfaced together; then, every block was compiled and simulated in order to obtain accurate results. The whole system was built to be functional, and finally, the frequency response was obtained. 100% significant accuracy and high quality are examined for implementing the filter in FPGA platform chip board programmed in (VHDL).**

***Keywords*—DSP, Electronics, Communication, FIR Filter, Computers, FPGA, VHDL**

I. Introduction

Recently, the field of Digital Signal Processing (DSP) has rapidly advanced. Moreover, Field Programmable Gate Array (FPGA) platforms are capable of reconfigurable design with respect to high-performance processing [1]. The designer is able to program the FPGA in accordance with the design specifications by employing Very high-speed integrated circuits Hardware Description Language (VHDL). For instance, audio processing is one application of the FPGA platforms. Hence, it will be presented later in this paper. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) goal is to minimize the size and cost of circuits as much as possible [2, 3]. The FPGA platform possesses various inexpensive multifunction components. Therefore, the circuit size has shrunk whilst the increase is being obtained in the performance. This section also introduces the FPGA board, VHDL language, Codec (WM8731) and Finite Impulse Response (FIR) filter. The digital filter's architecture [4] is mostly determined by the target applications to the particular implementations.

The remaining part of the paper is organized as follows. In sections two and three, the whole system will be described and explained in detail as three blocks design: Codec, S2P Adapter, and FIR filter. Then, the whole design is implemented, and the results are obtained.

Past research on the most prevalent published papers related to our study will be briefly surveyed and highlighted in chronological order.

First, many researchers worked to develop an FPGA design efficient multiplier, providing power and area efficiency [5–7]. For example, Llamocca developed in [8] a dynamically reconfigurable 2D filter bank that works with both real and complex-valued inputs, outputs, as well as filter coefficients. The system's efficiency was measured with respect to the accuracy, energy consumption, as well as processing time [8]. In 2017, Ryou and Simon presented a new applicable method to enhance the bandwidth by digitally cancelling acoustical resonances (poles) and anti-resonance (zeros) in the open-loop response via an FPGA FIR filter [9, 10]. In 2018, Pandey Kaur et al. studied and analyzed several factors like Off-chip, device power, junction temperature, thermal margin, and different dynamic power like Signal power, logic power, and DSP power. These may affect the energy efficiency alongside scaling down the output capacitance, where the latter verified better results [11]. While in 2019, Sumalatha et al. established Vedic Design - Carry Lookahead Adder FIR filter architecture to form the FIR filter operation with respect to Electro Cardiogram (ECG) signal de-noising application. The performance was evaluated using Verilog and Matlab [12]. In the same year, Mahabub implemented an FIR filter for the speedy detection of electroencephalogram (EEG) signal to compress and smoothen the signal [13]. In 2020, Thesni et al. concentrated on the occupied silicon area, resource usage, as well as design structure acquired for implementing FIR in FPGA [14]. In the same year, a paper was published on implementing DFT with low power consumption [15]. Here, Murali et al. implemented a 16 Tap FIR filter utilizing the Tree Algorithm, which satisfied

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well-defined results in terms of delay and utilization [3]. Furthermore, Datta and Dutta presented an IIR design based on a parallel–pipeline-based FIR filter in the same year. In comparison to conventional IIR filters, the suggested FIR-based IIR design provides higher operating speed, improved hardware utilization, as well as reduced power consumption [16].

A. FPGA

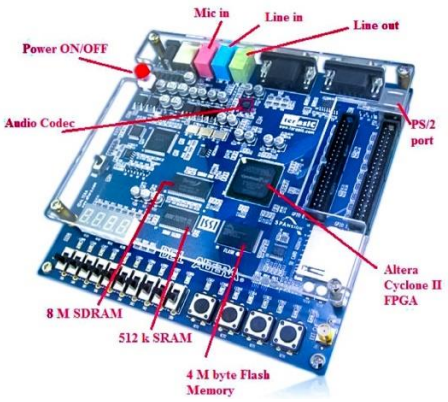

Figure 1. Altera DE1 board [1].

FPGA is an integrated circuit with a large number of chips whose internal function is denoted by the user [1, 17]. FPGA is based on user programming to conduct the necessary operation. FPGA has several applications, such as complex digital computations like speech recognition and audio processing, which possess greater performance computing. Meanwhile, Application-Specific Integrated Circuits (ASICs), in which only design can be built into the chip for one certain application, FPGAs are able to implement several applications many times by programming it according to the necessity. Cyclone FPGA family has several features, especially Cyclone II FPGA, which is used in the design of the whole project. It is the smallest size (0.13-µm), has the lowest cost, and the logic density is very high, up to (20,060) logic elements. This supports any design, specifically ones dealing with signal processing [18, 19]. The Altera DE1 board comprises the cyclone II FPGA and the Audio Codec, SRAM, SDRAM, and Flash memory, as shown in Fig. 1. FPGAs also provide the greatest gate densities and additional features, allowing them to have a large area to deal with multiple and different operations, specifically signal and image processing.

B. VHDL

VHDL is abbreviation for Very high-speed integrated circuits Hardware Description Language. It is used in processes and concurrent statements. “VHDL is a language for describing digital electronic systems” [4, 18, 20]. Its language consists of two main terms describing its structure. The first is an entity, while the second is architecture. While the former is used to define components, the latter contains the structure of all processes, which are described as their (behaviours) by the register transfer level of language (RTL). All these terms are a part of a specific library. It provides a wide area for the designers to simulate and obtain the outcomes for any design before implementing it with hardware. This leads to choosing the optimum design by refining different codes to the same design and testing them to end up with perfect results. Hence, VHDL plays a vital role in our project.

C. Codec (WM8731)

Codec (WM8731) is an integrated circuit *t* with low power stereo consumption. Its *c* has a built-in headphone driver that makes it work with MP3 audio, recorders, and other speech devices [2, 4, 18, 20]. The block diagram of Codec (WM8731) is shown in Fig. 2. It has two main interfaces, one called a control interface, and the second is a digital audio interface. Moreover, it has several I/O ports, such as the LLINEIN (Left channel Line Input) port, through which an analogue input audio signal will pass through it. The LHPOUT (Left headphone output) port on the opposite side is used to transmit the analogue audio signal out of the Codec chip. The digital audio interface has five I/O signals, which are: (Digital-To-Analog Connvertot Digital audio Data Input (DACDAT), Digital audio Bit Clock (BCLK), Digital audio Data Input Sample Rate Left Right Clock (DACLRC), Analog-To-Digital Sample Rate Left Right Clock (ADCLRC), and ADC-Digital audio Data Output (ADCDAT), which make Codec transfer the data to the FIR filter for processing through the S2P Adaptor block (as will be explained later). Meanwhile, the control interface (SCLK Serial Clock input/Output and SDIN Serial Data input/Output) will be used to initialize the Codec according to the I2C configuration protocol.

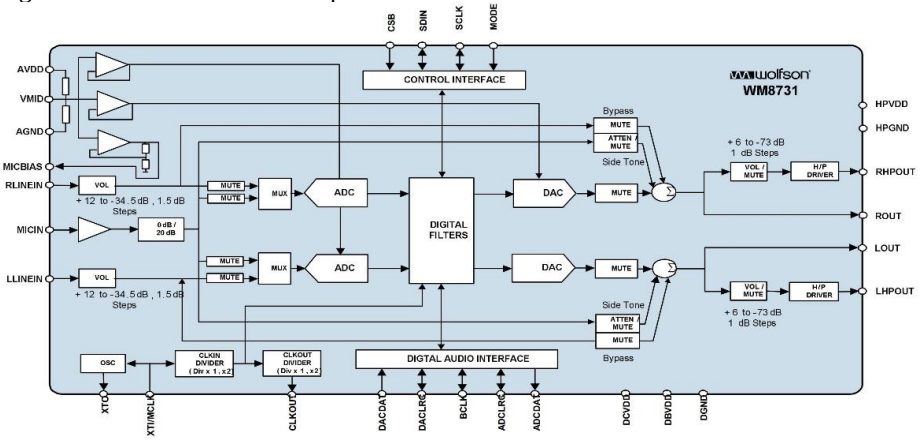

Figure 2. The block diagram of codec (WM8731) [20].

D. FIR Filter

The main idea of using the filter is to select a certain range of desired frequencies or reject unwanted frequencies. Generally, there are basically four types of filters which are: low pass, high pass, band pass, and band stop filters. FIR filter will be used in our project. FIR filter, in addition called a non-recursive filter, which is a digital representation of those four types. It can be designed to represent any one of them according to its transfer function and the coefficients [21, 22]. It is widely used in signal processing because $y(n)$ is the output of the FIR filter depending on the current and prior inputs. Therefore, it has a linear phase response. The equations below are for the transfer function, and the first relates $y(n)$ to $x(n)$.

$$y(n) = \sum_{k=0}^{N-1} b_k \; x(n-k) \tag{1}$$

$$\mathrm{H(z)} = \sum_{k=0}^{N-1} b_k \; Z^{-k} \tag{2}$$

According to the equations above, b_k represents the filter's coefficients. Furthermore, the symbol (Σ) implies the sum of the product coefficient with an input signal that experiences delay propagation. It is known as the tapped delay line, as illustrated in Fig. 3.

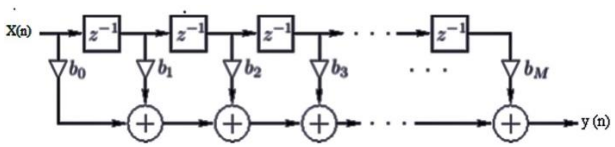

Figure 3. Logical schematic diagram of FIR filter [21].

II. METHOD

The whole system of the main three blocks is displayed in Fig. 4. The first block is a Codec initialization block, connected by a bidirectional connection with an S2P Adaptor, which is configured in both serial-to-parallel and parallel-to-serial modes. The third block is an FIR filter.

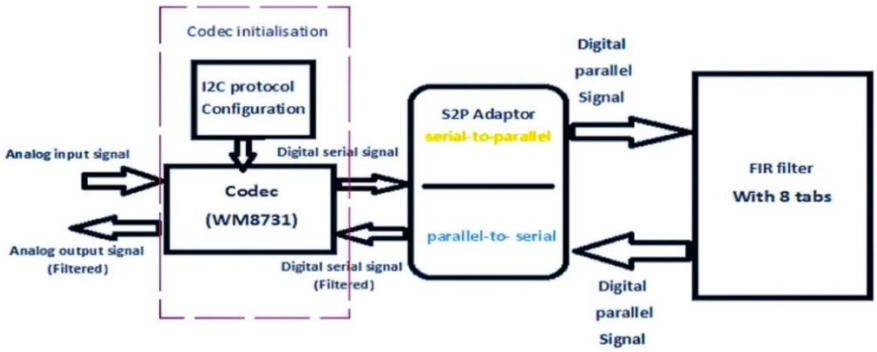

Figure 4. The whole FIR filter design.

Referring to the above diagram, processing (filtering) the audio signal is the main goal. First, the Codec is initialized, in which the I2C protocol configuration can be obtained. The former assists and organizes the transmitted bitstreams to the FIR filter after passing the S2P stage. In the S2P Adaptor block, there exist two steps. The first is to change the digital signal from serial mode to parallel mode, which is then sent towards the FIR filter. Here, the second step controls the flow of signal (bits stream) during the handshaking protocol. The output FIR signal must then be transformed to a serial signal using the same S2P block before being returned to the Codec.

A. Codec Initialization

The program's first step starts with the Codec block, where Codec does not work even though it turns the power button on. Therefore, the configuration clue of the Codec is to initialize it using the I2C protocol. This relies basically on SDIN and SCLK pins that work together. The first notation is to establish the start and end conditions of the transmission relating to the speed of the convenience clock, which is 100KHz and the rising edge of the master clock. After that, it should be sent byte by byte, but after every byte is transmitted, an acknowledgement should be received. To assure the data is received safely and correctly, the SCLK works on 500MHz. SDIN should be different at the start and stop, which means if the start condition is high in Eq. (1), the latter should be low, as shown in Fig. 5 with regards to the I2C protocol.

SDIN should load the data then transmit it out towards the FIR filter through the S2P Adapter, but this transmitting is actually controlled according to the I2C protocol, after choosing the start and stop and also loading the data inside SDIN. Hence, other steps should be achieved to complete the task perfectly. It begins with organizing the data as 7 bits as the chip address/codec address, 1 bit for Read/Write, 0 for writing, and vice versa. Moreover, 7 bits were arranged for the address of the register and the last 9 bits for register data. In fact, the total data consists of (11) words, and every word contains 24 bits. The data must start by sending MSB and LSB if the Codec did not receive ACK. Then, it will wait for the new start condition and resend it. Otherwise, if the ACK is received, it will keep going on sending each word until finishing all words, and the stop condition will appear.

This is to know the mechanism of the codec operation through the I2C protocol by having a look inside it. Actually, after initializing the Codec, it has two-wire according to I2C. Codec by I2C protocol has various options, giving the designers a wide area to deal with it according to any design.

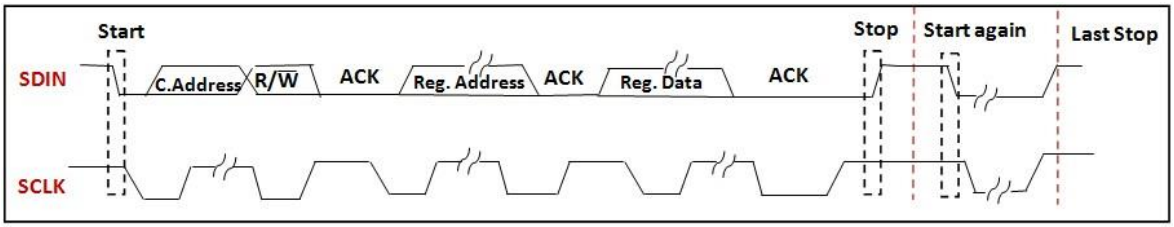

Figure 5. I2C protocol [4].

B. S2P Adaptor Block

The primary function of this block is to change the Codecs data from serial to parallel and pass it to the filter block. Subsequently, the conversion is repeatedly inversed, where the filtered parallel data from the FIR block transforms into a serial data format and feeds to the Codec block. In addition, two interfaces will be obtained to achieve the S2P purpose, which are a digital audio interface and paralleling interface (which will be demonstrated later), as shown in Fig. 6.

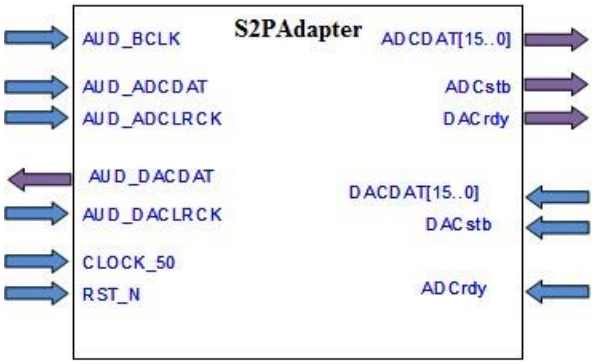

Figure 6. Block diagram of S2P Adapter.

C. FIR Filter Block

As mentioned and described in FIR filter in detail, the main equations (1) and (2) represent the design of FIR filter.

To complete the design, we just need to know the number of tabs (N) and the values of coefficients. Therefore, the specifications are declared, which means the coefficients are (-1260, 7827, 12471, 16384, 16384, 12471, 7827, -1260). As a result, the FIR filter's complete equation may be expressed as Eq. (3):

$$[y(n)= -1260\ x(n) + 7827\ x(n- 1) + 12471\ x(n- 2) + 16384\ x(n- 3) + 16384\ x(n- 4) + 12471\ x(n- 5) + 7827\ x(n- 6) + -1260\ x(n- 7)\ ] \quad (3)$$

The FIR Data shifter filter comprises seven stages, in which every step resembles a 16-bit register. Moreover, the design requires a multiplier, using either eight multipliers or one. Here, the sampling is not faster than a multiplier, and the design might become more complicated. As a result, a one multiplier is utilized to multiply the coefficients of the FIR by the output of every 16-bit register from the data shifter (accumulator), as illustrated in Fig. 7. In the operation of multiplying each multiply coefficient with one input (16 bits), we will obtain one shift to the right, so overall will result in 8 shifting from 8 tabs multiplied with the 8 input audio data. This means the size of the accumulator should be (35) bits from (32bits +2^3), and after the final result, it could discard the 19 bit in the least significant and pick the most 16 bits only.

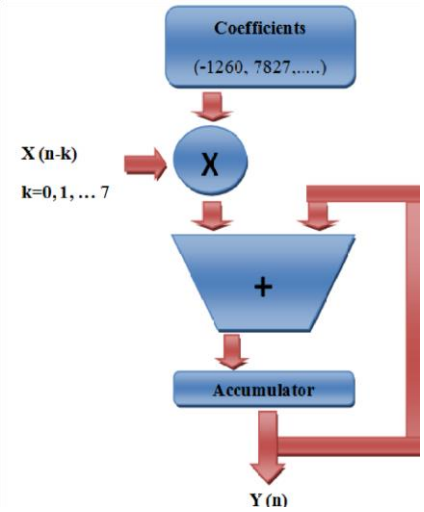

Figure 7. The concept of FIR design.

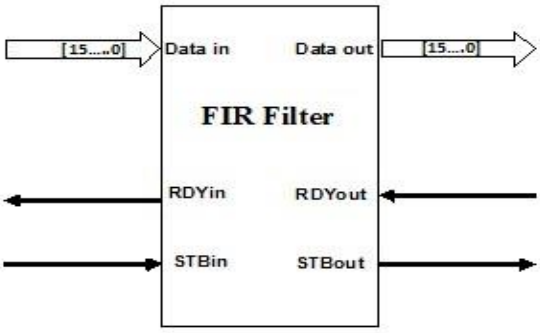

Figure 8. Strobe/Ready Handshaking (Parallel Interface).

According to the normalized frequency response, it can be considered that the FIR filter has a low pass feature. Therefore, the input parallel signal will pass through it as long as the area of pass band frequency starts with stopping at a cut-off frequency that is approximately 9 kHz.

1) Parallel interface

It is essential to make the S2P block work properly with the FIR filter. To achieve that aim, synchronization must be accomplished between the signals of the S2P and the receiver of the FIR filter to avoid losing the data. The Handshaking technique is employed to achieve synchronization. The Strobe and Ready signals are the main components of this approach. Fig. 8 below shows the handshaking technique.

As mentioned, the Handshaking technique depends on the strobe and Ready signal to achieve the synchronization. Therefore, these two signals play a significant role between FIR blocks and S2P. Specifically, the Strobe signal implies that there is the input pin of the S2P in the data packet (16 bits) and is ready to deliver it to the FIR. Meanwhile, the Ready signal states that the receiver (the S2P) can receive the data packet or is busy to avoid missing it.

III. Results and Discussion

A. Codec Initialization Block

As mentioned before, the I2C protocol plays the main role in initializing the Codec. In particular, the SDIN and SCLK are manipulated to be compatible with the desired design. Returning to the specifications of the Codec, the first change is the speed of the main CLK. The main Codec frequency (CLOCK_50) works on 50 MHz while SCLK works on 100 kHz. Hence, the frequency divider signal (f_div) is used to slow the main clock by making the f_div counter count down from 499 to 0 (500). That counter will delay the main clock 500 times, resulting in SCLK being equal to 100 kHz, simply dividing the main clock frequency by SCLK frequency as (50r×106/100×103=500). The Final simulation of the codec should be as in Fig 9

On the other hand, the BCNT (bit counter variable) counter is used to represent one word of the data bits stream. It counts down from (28 to 0), which allocates 24 bits of the data, 3 for acknowledgement, and 2 for start as stop conditions. Thus, the 29 bits representing the BCNT counter will be counted 11 times according to the 11 words. The result of that is shown in Fig. 11.

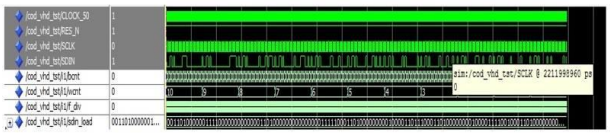

Figure 9. Final simulation of the codec.

The 3 acknowledgement bits as shown in Fig. 10, are crucial to assure that the data, whether received from the Codec or not, gives the design the ability to debug it again. The SDIN signal will indicate 'Z' during these bits (19th, 10th, and 1st).

Figure 10. I2C Protocol with declaring ACK.

B. S2P Adapter Block

The S2P Adapter block contains two channel. The first is the input channel which receives the packet data in a serial format. On the other hand, the second is the output channel that feeds the Finite Impulse Response (FIR) data packet in parallel format. That shows the vital role of the S2P in adapting the data packet format according to the specifications of the design. In addition to that, the S2P uses the same output channel to receive the processed data obtained from the FIR filter, converts the data from parallel to serial, and sends it to the Codec chip. The two important signals are BCLK and LRC, which conduct the transition and specify the beginning of the transmission between the input against the output. The whole code is written in the Appendices. The Input and Output channels with respect to the S2P Adapter are shown in Fig. 11 below:

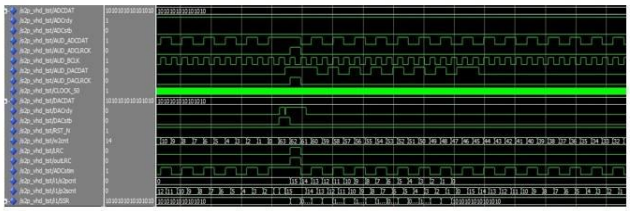

Figure 11. The input and the output of the S2P adapter.

C. FIR Filter Block

The FIR filter represents the backbone of the project. To explain it further, when the input of the S2P gets a data packet to be sent to the filter, the STBin signal is set to high (1). Concurrently, when RDYin signal is low (0), that means the handshaking is achieved, leading to a set-up linking the two blocks. In contrast, if RDYin is high in Eq. (1), indicating that the FIR filter is busy, we wait for a while after the processing is finished, and then RDYin will be set to be (0). Similarly, the other side has the same procedures of the protocol when the processed data of the FIR filter block is prepared to be sent back to the S2P Adapter.

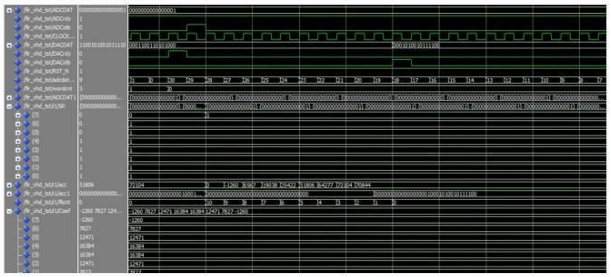

Figure 12. The simulation of the FIR.

D. Hardware Test

This stage combines all three blocks together to obtain the final design. In addition, we used some auxiliary blocks like Codec clock (generator) and Synchronous blocks, as illustrated in Fig. 13. Synchronous blocks communicate between two different devices that have different clocks. Finally, the final project is ready to be downloaded to the DE1 board.

The SignalTap II logic Analyzer is used to capture the internal digital waveform, especially since some signals like BCLK and CLOCK_50 change. For instance, the BCLK is used to detect the ADCDAT and DACDAT. In Fig. 14, the input signal is represented with left and right channels, while the output is designed to capture just the left channel. ADC strobe is not shown in this figure

because it is a short signal, and it is much shorter than BCLK. In order to capture the short signals, the CLOCK_50 should be used as a reference signal, but this leads to running out of memory very soon.

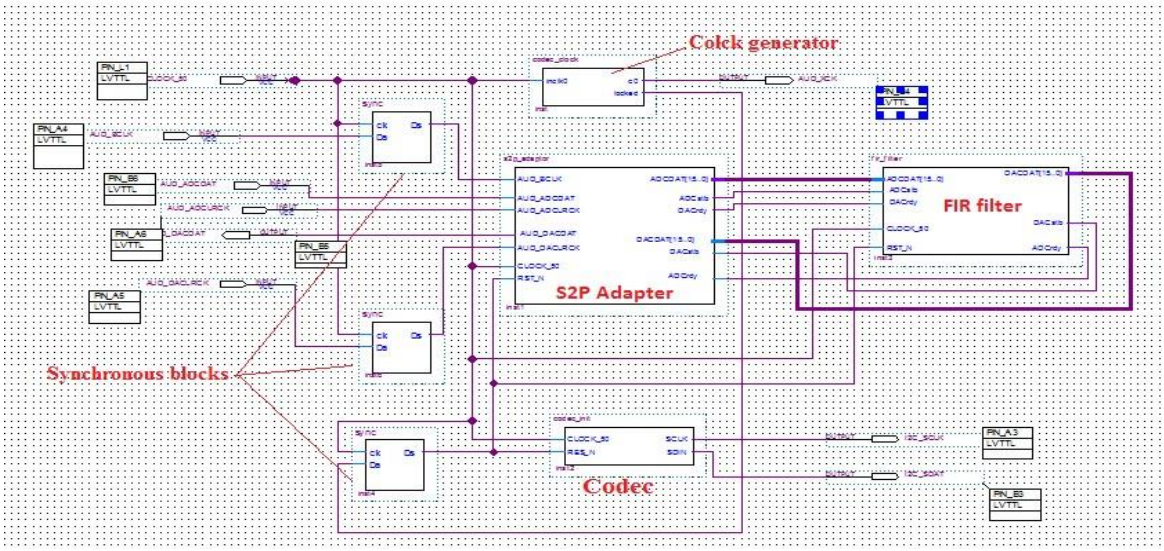

Figure 13. The system architecture [18].

Figure 14. Signal Tap II logic analyzer.

The input sine wave signal is generated with various frequencies by generator. The oscilloscope is also employed to calculate the ultimate signals. The input signal is linked to the DE1 board via the LINEIN port to evaluate the FIR filter in a real-world setting. The output port (LINEOUT) is linked to an oscilloscope, and the frequency response of the FIR filter may be observed by altering the input signal frequency, as illustrated in the accompanying images.

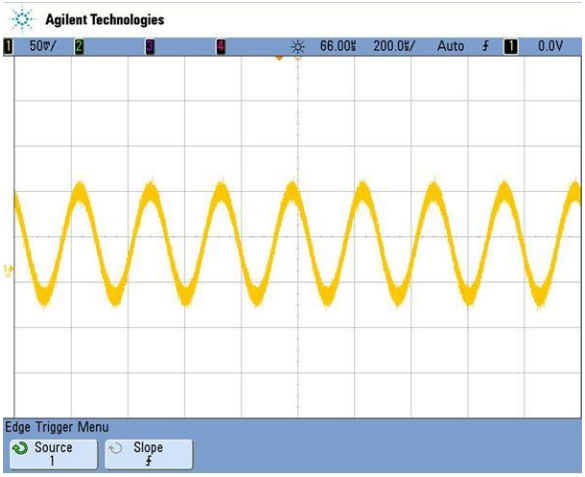

Figure 15. 5 kHz signals (input and output).

In Fig. 15, it can be easily observed that the output signal's frequency is less than or equal to 5 kHz and is approximately the same compared with the input signal. Meanwhile, when it is gradually increased, the output will be experienced from the attenuation even become equal to or larger than 9 kHz. This is because the output's cut-off frequency will be filtered out, as shown in Figs. 16-17.

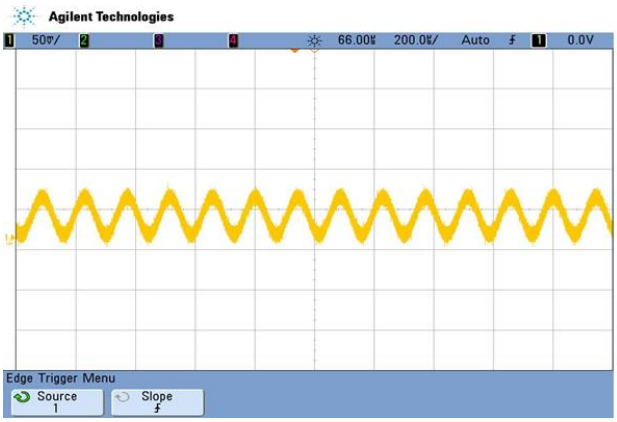

Figure 16. The output at 7 kHz.

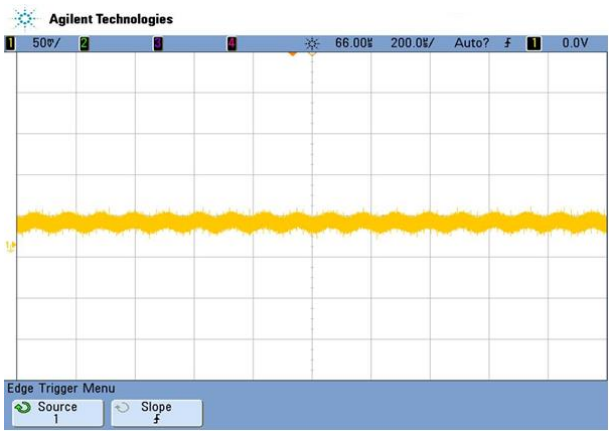

Figure 17. The output at 9 kHz.

The sweep sine is utilized at the input to acquire the entire frequency range of the audio signal. As a result, the

FIR low pass filter frequency response is easily visible, Fig. 18.

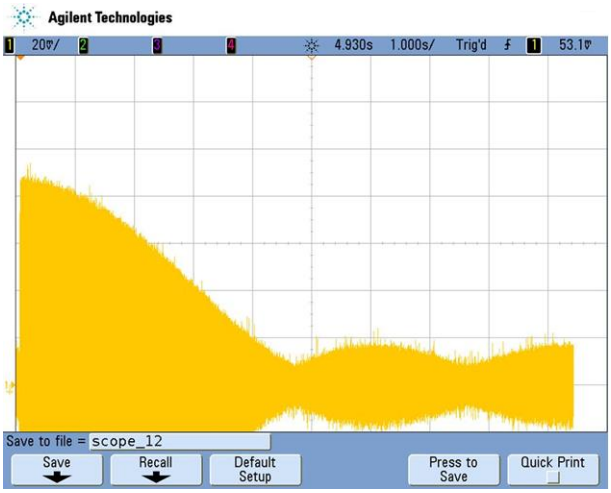

Figure 18. The output of sweep sine wave (100 Hz to 20k Hz).

IV. Conclusion

In conclusion, the audio Finite Impulse Response (FIR) filter has been effectively carried out on FPGA. Because of the strong countenances of VHDL to split the whole design to more than one, it was used to create the FIR filter. The entire project was initially classified into three blocks: Codec initialization, S2P adapter, and FIR filter. In order to govern the transmission of data in the Codec initialization block, the I2C protocol is employed, which comprises the necessary configurations. The start bit was detected, and then the 1st word (24 bits) was conveyed till stop bit was revealed. Because of the large number of data words used, this method was performed eleven times. Furthermore, the Codec received an acknowledgement after every 8 bits of transferred data to check that the Field Programmable Gate Array (FPGA) received the configuration data successfully. The input channels of the S2P Adapter block and the output are separate. The digital data is converted from serial to parallel before being passed to the FIR filter through the input channel. The data was 16 bits, which corresponded to the Codec's left channel. This is accomplished by transmitting first the MSB (15), followed by the remaining bits. The parallel data from the FIR block has been transformed into serial data by the output channel. The FIR filter is the third block. To produce the final filtered audio signal, this block was built using a shifter and an accumulator. The values were mixed inside the accumulator after multiplying each shifter output (16 bits) by its associated coefficient. Finally, the S2P Adapter block received the 16 bits of collected data (31 down to 16) from the FIR low pass filter. In addition, the primary three components were concatenated to create the entire filter. To complete the architecture, further blocks such as the Codec clock block and synchronous blocks are included. These extra blocks can be found in the library. The next step was to clean up the final design and upload it to the DE1 board. A sine wave with various frequencies was utilized as input in the hardware test. As a result of the low pass filter's action, the output signal decreases as the frequency increases. A test bench is advised to be written to ensure that any programme is working appropriately.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

M. A. conducted the research; H. A. analyzed the data; A. A. wrote the paper. All authors had approved the final version.

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